FD-SOI: A technology setting new standards for IoT, automotive and mobile connectivity applications
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Introduction
Fully depleted silicon-on-insulator (FD-SOI) is the only technology bringing together three substantial characteristics of CMOS transistors: a 2D planar transistor structure, fully depleted operation and the capability to dynamically modify the threshold voltage of transistors after manufacturing. It relies on a very unique substrate whose layer thicknesses are controlled at the atomic scale.

FD-SOI offers remarkable transistor performance in terms of power, performance, area and cost tradeoffs (PPAC), making it possible to cover low-power to high-performance digital applications with a single technology platform. In addition, FD-SOI has numerous unique advantages including the ability to mitigate process, temperature, voltage and aging variations through body bias, near-threshold supply capability, ultra-low sensitivity to radiation and very high intrinsic transistor speed, making it most likely the fastest RF-CMOS technology on the market.

These attributes make FD-SOI a fantastic integration platform that combines high-performance and ultra-reliable digital blocs with outstanding RF characteristics, all in a very limited cost and power envelope. FD-SOI has set new standards in many applications including the Internet of Things (IoT) with ultra-low-power Nb-IoT devices with integrated RF, automotive systems from vision processors for ADAS to infotainment, and mobile connectivity from 5G smartphones to wearable electronics.

FD-SOI technology is supported by multiple foundries and integrated device manufacturers (IDMs) with full technology offerings now available for the 65-nm, 28-nm and 22-nm nodes and emerging for the 18-nm and 12-nm nodes. With this global ecosystem in place, FD-SOI is ready for applications development for diversified markets.

At the heart, a unique substrate
Everything in FD-SOI technology starts with the substrate. It directly defines the transistor architecture, as shown in Figure 1. To allow the fully depleted operation of transistors, the thickness of the top silicon layer defining the device channel must be tightly controlled, with the thickness target typically around 60 Å or 11-22 atomic layers. Given the consumption of silicon material during device fabrication, foundries usually require a 120 Å incoming top silicon specification.

Uniformity is another very challenging specification needed to keep transistor variability as low as possible. Uniformity of +/-5 Å or 2 atomic layer is typically considered essential. The buried oxide (BOX) layer also must be very thin – around 20 nm – to maximize electrostatic control in the transistor channel due to the ground-plane effect.
Manufacturing a 300-mm piece of crystalline silicon with a thickness specification as low as 11 +/- 2 atomic layers is understandably difficult. Ten years ago, it sounded unachievable, so people studied other paths to enable fully depleted transistors [1]. This dream is now reality on an industrial scale thanks to the well-known Smart Cut™ process.

**Simpler manufacturing despite a more complex substrate**

With standard technologies, getting more performance out of silicon below the 28-nm node means adding greater complexity to the manufacturing process. Consequently, the smaller nodes get, the more masks are needed to create chips. This increases manufacturing costs as well as other non-recurring engineering costs including design flow, design verification, mask sets and more. On the other hand, FD-SOI uses a simple manufacturing process. In fact, it offers more performance while decreasing manufacturing complexity. Most of the channel engineering work is done directly at the substrate level, making FD-SOI easier to implement than bulk silicon, as major foundries have reported [2] [3].

**Key features**

**Fully depleted transistor operation gives superior power/performance tradeoff**

All CMOS technologies below 22 nm require fully depleted operation of transistors. This is done by directing the current flow from source to drain through a very narrow channel, typically less than 6 nm. With FinFET devices, this channel is defined vertically using lithography. With FD-SOI, the channel is defined horizontally by stacking a very thin silicon layer on top of a very thin BOx layer using the Smart Cut process described above.

Fully depleted operation helps to dramatically decrease short channels effects. Consequently, no dopant is required inside the channel. This drastically reduces the variability of transistor characteristics while increasing transistor mobility. FD-SOI transistors also benefit from improved junctions with less capacitance thanks to the BOx.
Mitigating variations through body bias

Another advantage of FD-SOI is that it enables body biasing. FD-SOI’s thin BOX not only enhances electrostatic control of the channel, but also makes it possible to completely tune the threshold voltage through back biasing. Low, mid-range and high $V_{th}$ can be achieved simply through back-gate polarization (Figure 2). The thin BOX behaves like a second gate and, most importantly, it can be used dynamically.

Body bias can be used to:

- Compensate for static process variations after manufacturing and during design phases
- Compensate for dynamic temperature and aging variations after manufacturing and during design phases
- Achieve a minimum energy point for each power mode
- Boost performance at maximum $V_{dd}$

Figure 3: Process compensation principle. Body bias helps to offset process variation after manufacturing (1) and also helps to achieve better PPA metrics during design steps by significantly tightening design corners (2).
Contrary to supply voltage scaling techniques, which is another technique for process compensation, body bias offers these very unique benefits:

- Body bias has no impact on reliability (NBTI and oxide breakdown) [5].
- Process compensation with body bias does not consume any supply voltage budget, giving more room to boost performance at maximum $V_{dd}$.
- Body bias can be applied on NMOS vs. PMOS selectively.
- Body bias does not require an external voltage regulator. Embedded body bias generators can be used with almost no impact on space and power constraints.
- Body bias is extremely efficient in compensating for $V_{th}$ variations induced by temperature and aging effects.
- Body bias compensation is very easy during early design phases, allowing reduced margins for process, temperature and aging.

Body bias is a very powerful knob in automotive applications. Significant reductions in process variation can be achieved (Figure 4), making it easier for product engineers to guarantee product specifications at the 1-ppm reliability level. Dynamic reliability drift compensation is another very promising topic, which could lead to totally resilient systems [6].

![Figure 4: Body bias process compensation principle applied on ADAS chips. A significant reduction of process spread can be achieved at the product level [7].](image)

**Outstanding analog/RF characteristics**

With bulk technologies analog/RF designers must make their designs work with increasingly degraded transistors as linewidths shrink. Meeting speed, noise, power, leakage and variability requirements is becoming more difficult. With FD-SOI, transistors benefit from improved matching, gain and parasitics, greatly simplifying analog and RF circuit design [8]. Body bias also has potential for the design of many new analog/RF structures [9].
Integrating as many analog/RF functions as possible into a single RF-CMOS silicon platform is becoming more important in many markets for obvious cost and power reasons. But RF-CMOS platforms have a limited ability to increase frequency, especially in the mmWave spectrum (30 GHz and above). This is a bigger issue with 3D devices such as FinFETs, which must carry very strong parasitic capacitances due to their 3D structures [10]. As a result, SiGe-Bipolar platforms are often used for this frequency range. FD-SOI is a planar technology so it does not have the limitations of 3D devices. $F_t/F_{\text{max}}$ in the range of 325 GHz to 350 GHz has been reported [3], allowing full usage of the mmWave spectrum up to 100 GHz and giving FD-SOI RF-CMOS platforms a bright future in many applications including 5G and automotive radars.

Associated with a high-resistivity base substrate, FD-SOI has the potential to combine low loss, low crosstalk and high linearity components with high switching frequency capabilities. This enables completely new RF system-on-chip (SoC) devices for the next generation of wireless communication by integrating front-end module components such as switches, power amplifiers and low-noise amplifiers with mmWave transceivers and high-performance digital blocks.

**Using ultra-low voltage**

Almost all CMOS technologies achieve their best energy efficiency – i.e., the lowest amount of energy per function, regardless of the frequency – at around 0.4 V supply voltage, often referred to as $V_{\text{dd}}$ [11]. At this level of supply voltage, variability management is a real challenge. Thanks to body bias and its intrinsic low-variability characteristics, FD-SOI can achieve very low supply voltages. More generally, the ability to lower the supply voltage, although not necessarily as low as 0.4 V, can be difficult in applications in which power is a greater challenge than performance. Given that dynamic power scales with $V_{\text{dd}}^2$, FD-SOI’s ability to use a much lower supply voltage presents a unique advantage.

**Radiation immunity**

Low sensitivity to high-energy particles is another key characteristic of FD-SOI. High-energy particles can interact with silicon and generate a significant amount of charges capable of flipping the transistor logic state, thus increasing the soft error rate (SER). FD-SOI devices are completely isolated from the substrate by the BOX layer so any charge generated in the substrate is unlikely to modify the device logic state. In short, FD-SOI is much less sensitive to SER than bulk devices [12]. This has very important consequences for safety-critical devices such as autonomous car systems or low earth orbit (LEO) satellites.

**FD-SOI benefits for different applications**

All these attributes make FD-SOI a vital technology for a very large range of applications.

In the mobile space, FD-SOI can bring highly integrated solutions for application processors, basebands and transceivers with unique power, performance and cost tradeoffs for the mainstream market. Imagers can take advantage of its very low power envelope to position the image-signal processor in stacked logic very close to the sensor.

In automotive applications, vision processors for ADAS and infotainment represent key markets for FD-SOI, where it provides huge differentiation in terms of reliability and power consumption, enabling highly reliable fanless solutions. As an example, the new generation of ADAS processors from Mobileye, a world leader in vision and artificial intelligence, is based on 28-nm FD-SOI technology. The EyeQ®4 is a chip-
based vision-assistance system that is currently available with calculating performance eight times superior to its predecessor.

Another example comes from NXP Semiconductors, which announced in March 2017 the first application processors based on 28-nm FD-SOI technology [13]. These i.MX 8X processors are intended for embedded applications used especially in the automotive and industrial sectors. They provide high reliability, which is essential in these two markets.

In IoT applications such as medical devices, wearable electronics, home assistants, edge computing and narrow-band and short-range communications, FD-SOI’s intrinsically better channel electrostatic control and its ability to operate at low voltage can enable significant gains in battery life – or even completely battery-less solutions – along with the best cost per transistor of all CMOS technologies. A good example is Sony’s GPS product, which reduces power consumption 76 percent by using FD-SOI technology (Figure 5) [14].

In April 2016, the AMAZFIT sports smartwatch by Huami achieved record-high energy efficiency as the first electronic product to use this new GPS made with FD-SOI technology [15]. With the GPS activated, the smartwatch can be used continuously for 35 hours – a battery life that is two to five times longer than that of similar watches on the market.

More devices will benefit from FD-SOI in the future. Using body-bias capabilities to compensate for temperature and process variations, FD-SOI has the potential to enable extremely power-efficient devices, as already demonstrated by the French Lab Leti [16]. Combined with new low-power embedded non-volatile eMRAM memories, FD-SOI will open up new perspectives for a wide range of products. ARM recently announced an eMRAM compiler using Samsung’s 28-nm FD-SOI technology that is capable to replacing flash memories and part of cache memories [17]. NXP Semiconductors, Renesas, STMicroelectronics and Lattice are among the companies fully committed to the technology for this application range.
In RF, FD-SOI has great potential for communication protocols with frequencies both below and above 6 GHz. Satellite transceivers, wi-fi/Bluetooth combination chips and 4G/5G transceivers can benefit from the intrinsic higher behavior of the technology in analog/RF devices on many key metrics. Compared to bulk technologies, FD-SOI enables significantly lower power consumption. In March 2017, Eutelsat and STMicroelectronics announced a low-power, low-cost SoC solution for interactive satellite terminals [18]. This 28-nm FD-SOI system is currently the most energy efficient SoC available. For communication protocols with frequencies in the mmWave spectrum (typically up to 80 GHz) such as 5G or automotive radar, FD-SOI can be an exceptional platform to integrate front-end modules with transceivers and digital blocks to provide cost-effective 5G solutions.

The performance advantages enabled by FD-SOI are expected to bring dynamic advances in other areas as well, including artificial intelligence, bitcoin mining and display controllers. That potential is confirmed by GLOBALFOUNDRIES, which announced recently that the company’s 22-nm FD-SOI (22FDX®) technology has already delivered more than two billion dollars in revenue for client design wins [19]. With more than 50 total client designs, 22FDX is proving to be the industry’s leading platform for power-optimized chips serving the automotive, 5G connectivity and IoT markets.

Manufacturing capacity and roadmap
Today, FD-SOI technology is offered by two of the world’s top four foundries. It is available for production in 28 nm (Samsung) and 22 nm (GLOBALFOUNDRIES). The 18-nm and 12-nm nodes are in development by Samsung and GLOBALFOUNDRIES, respectively. All nodes proposed by foundries have, or will have, RF and embedded non-volatile memory options.

Faced with the market’s growing interest in FD-SOI, GLOBALFOUNDRIES announced in February 2017 plans to expand the capacity of its Fab 1 facility in Dresden by 40 percent by 2020 as well as a strategic partnership with the Chengdu municipality to build a 300-mm fab to support the growth of the Chinese semiconductor market and to meet accelerating global customer demand for 22FDX [20].

Two IDMs, STMicroelectronics and Renesas, also have their own FD-SOI technology. STMicroelectronics adopted FD-SOI technology in 2012 [21] and started several projects. The company demonstrated an ARM-based application processor for smartphones with 3 GHz+ operating frequency on 28-nm FD-SOI [22]. The technology is now used at STMicroelectronics for many diversified markets [18] [23]. Renesas has a 65-nm version of FD-SOI called silicon-on-thin-BOX (SOTB), which targets ultra-low-power MCU markets. Renesas has reported very low power consumption with this platform, as small as a tenth of that achieved using bulk silicon [24].

Regarding substrate manufacturing capacity, Soitec decided in September 2017 to re-open its Singapore fab to meet increasing customer demand and to provide multi-site FD-SOI substrate sourcing to the global semiconductor market [25]. Combined with its fab in Bernin, France, Soitec will be capable of ramping up to 1.5 million FD-SOI wafers per year. The company has plans to go beyond that to meet additional customer demand.

Conclusion
Growing interest in FD-SOI reflects today’s new paradigm for semiconductor technologies. Customers are demanding more computing capability with drastically reduced power consumption, enabled by
enhanced analog/RF integration. With its unique characteristics, FD-SOI is generating increasingly strong interest from major players in the semiconductor ecosystem for a very wide range of markets. FD-SOI is now a mainstream technology, which device designers are leveraging for key competitive advantages.

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References


**About the author**

Manuel Sellier is Soitec’s Product Marketing Manager responsible for defining the business plans, marketing strategies and design specifications for the FD-SOI, Photonics-SOI and Imager-SOI product lines. Before joining Soitec, Manuel worked for STMicroelectronics, initially as a digital designer covering advanced sign-off solutions for high-performance application processors. He earned his Ph.D. in the modeling and circuit simulation of advanced MOS transistors (FD-SOI, FinFET). Manuel holds several patents in various fields of engineering and has published a wide variety of papers in journals and at international conferences.