Early-Stage RTL Power Estimation and Exploration

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Today's Significant Power Issues

Power Budget of Chip

- Is power consumption on target?
- Is the RTL within the power intent?
- Are chips failing in production?

Power Management Strategies

The number of transistors in a microchip doubles every two years, emphasizing the importance of early-stage power exploration.

Designers can no longer hold up until the end-most netlist to get accurate power numbers.

Reduce the power in design?

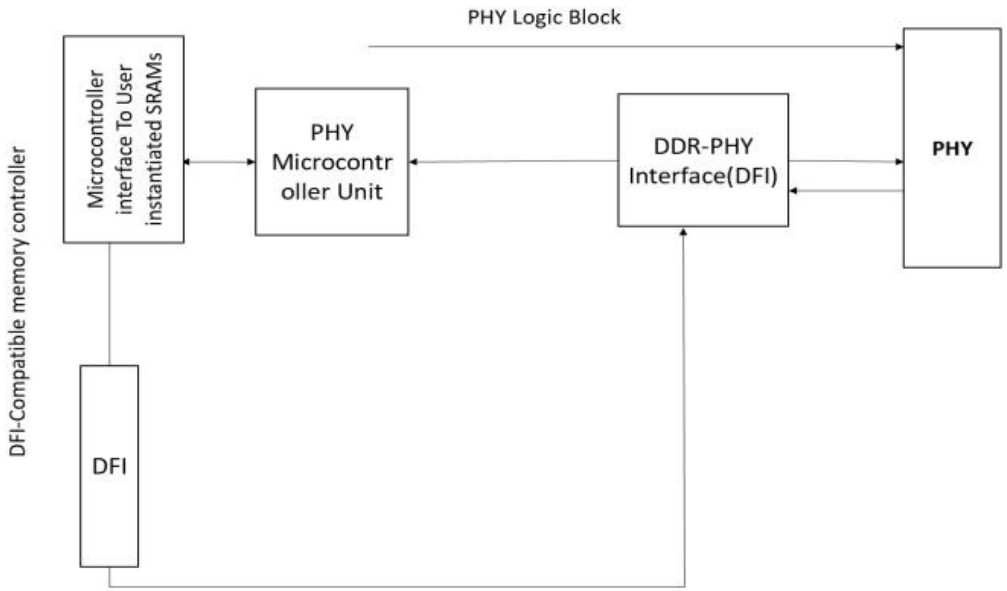
- Identify power loopholes ?
- Identify the correct techniques ?
- How RTL should be modified to have the most impact ?

Introduction

- Every milliwatt of power counts, regardless of the application. The overall power of a Silicon on Chip (SoC) architecture is mainly composed of its dynamic and static power components.
- Dynamic power is the amount of power utilized by a device as the signals vary.
- Static power is associated with the power dissipated when the transistor is in an idle state.
- The Low-power design can be studied at different levels, including the logic, circuit, device levels, and system architecture.

Introduction (Contd.)

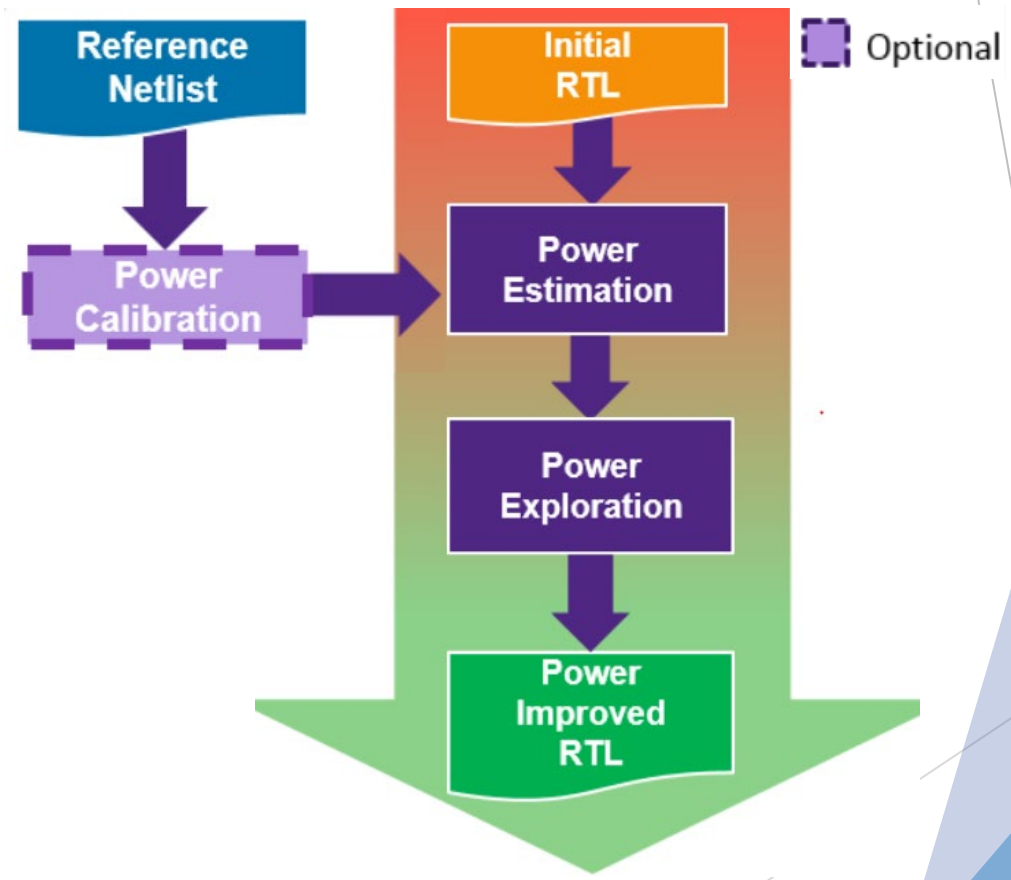
- In the view of the fact that the engine can utilize most of the cells in the given target libraries, it can provide a reliable starting point for power calculation.
- The analysis in this research has been done on the dual data rate physical interface (DDR-PHY) IP.
- The PHY can operate in various modes depending on the input/output ports.



A high-level diagram of DDR-PHY

Introduction (Contd.)

- There are four critical components for estimation and reduction, as indicated, to tackle all elements of power analysis, including early RTL estimation and exploration.
  - Power Estimate
  - Power Exploration
  - Power Reduction
  - RTL Power Sign-Off

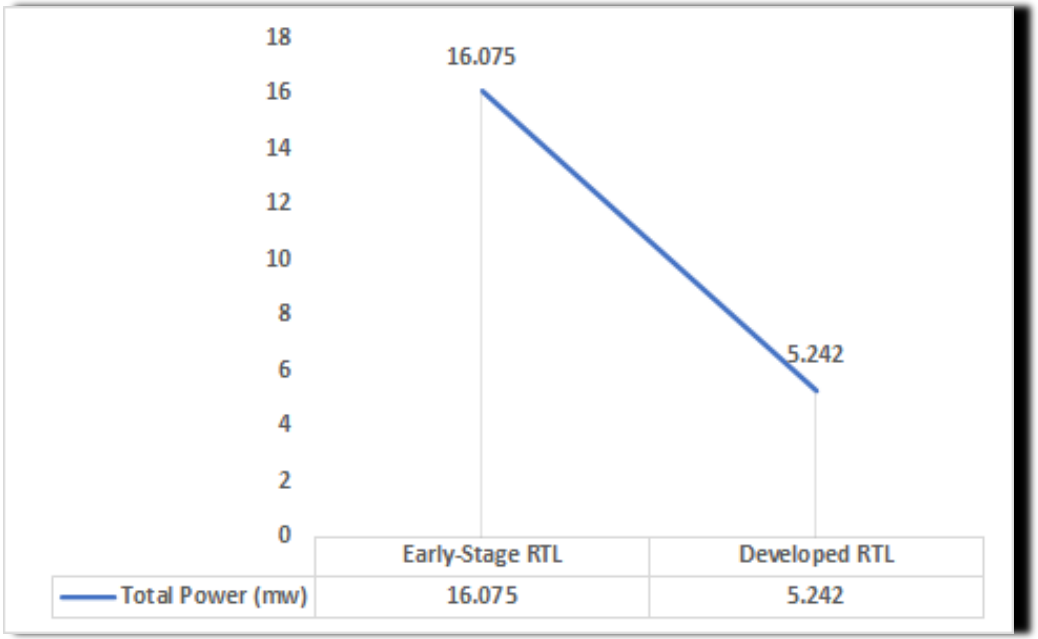


Problem Statement

- The study here is restricted to the low power state of PHY. PHY Fast Standby/Low Power (LP2) allows the SoC to save the maximum power while the DRAM is in a Self-Refresh mode.
- As the LP2 stage expects to have the maximum power saving, it is required to maintain a low power criterion. This problem, indeed, will not be achievable by the conventional methods of power estimation as it requires a finalized netlist.
- However, waiting for the stable RTL for the LP2 stage raised concerns about the turnaround time and expectations led to the notion of RTL power exploration at an early stage.

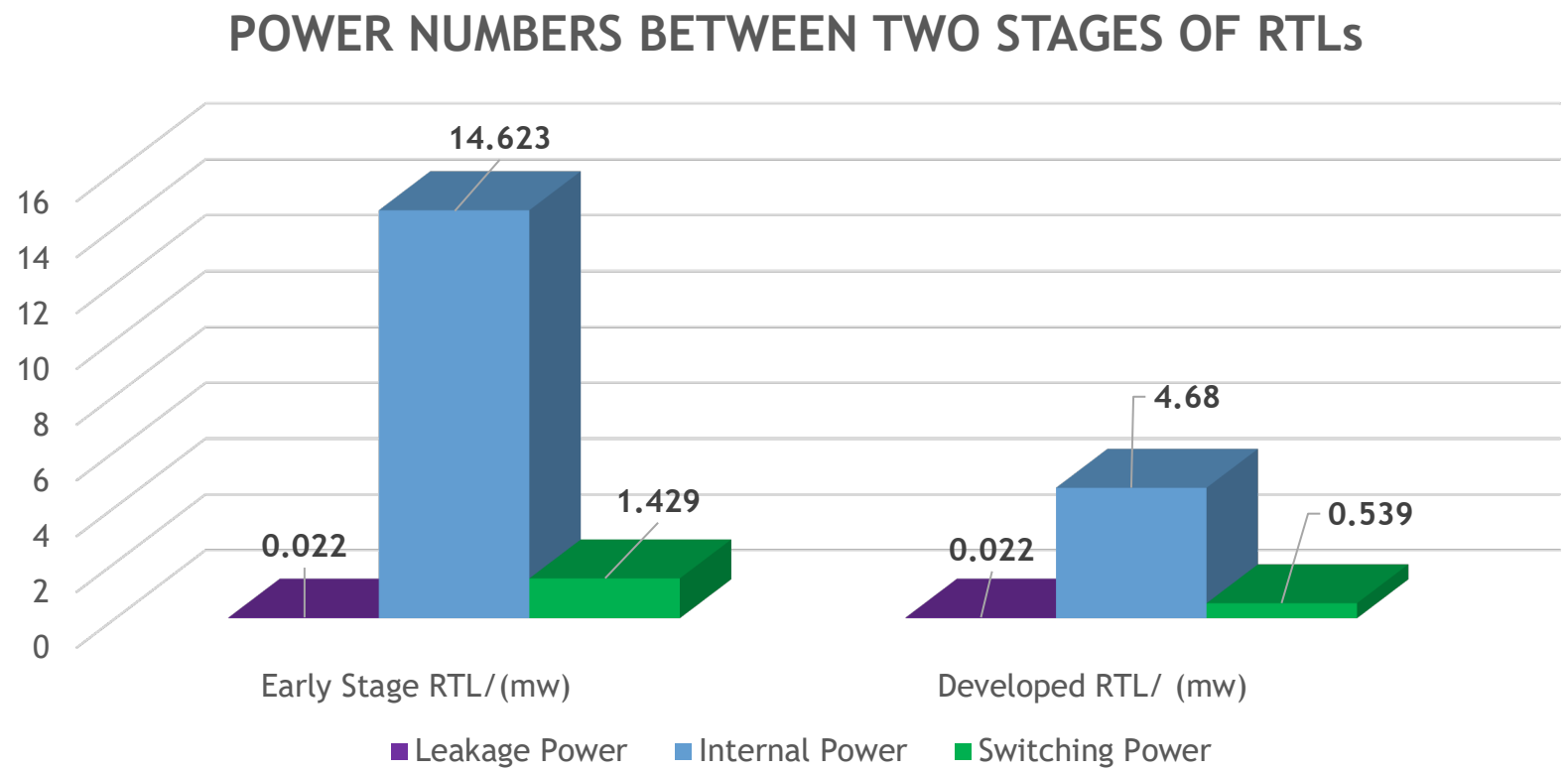
Problem Statement (Contd.)

- The results of the Early-Stage RTL, on the other hand, exceed the power specifications. The efficacy of the developed RTL is achieved by analysing every statistical element of RTL.
- Since a design's power is a consequence of how it conducts a calculation over time, practically all of the crucial alterations that significantly impact a design's power are sequential—they alter the sequence of values created at key internal registers or memories over time.

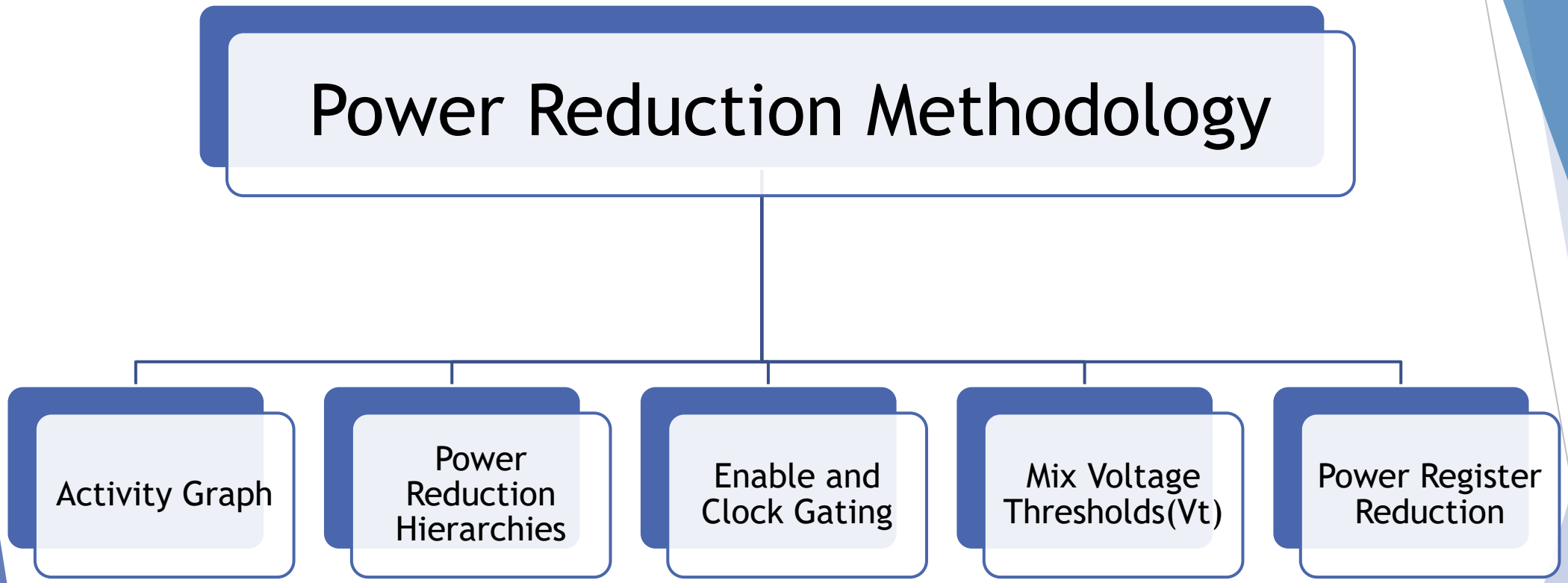


Power estimates at different RTL stages

Results of LP2

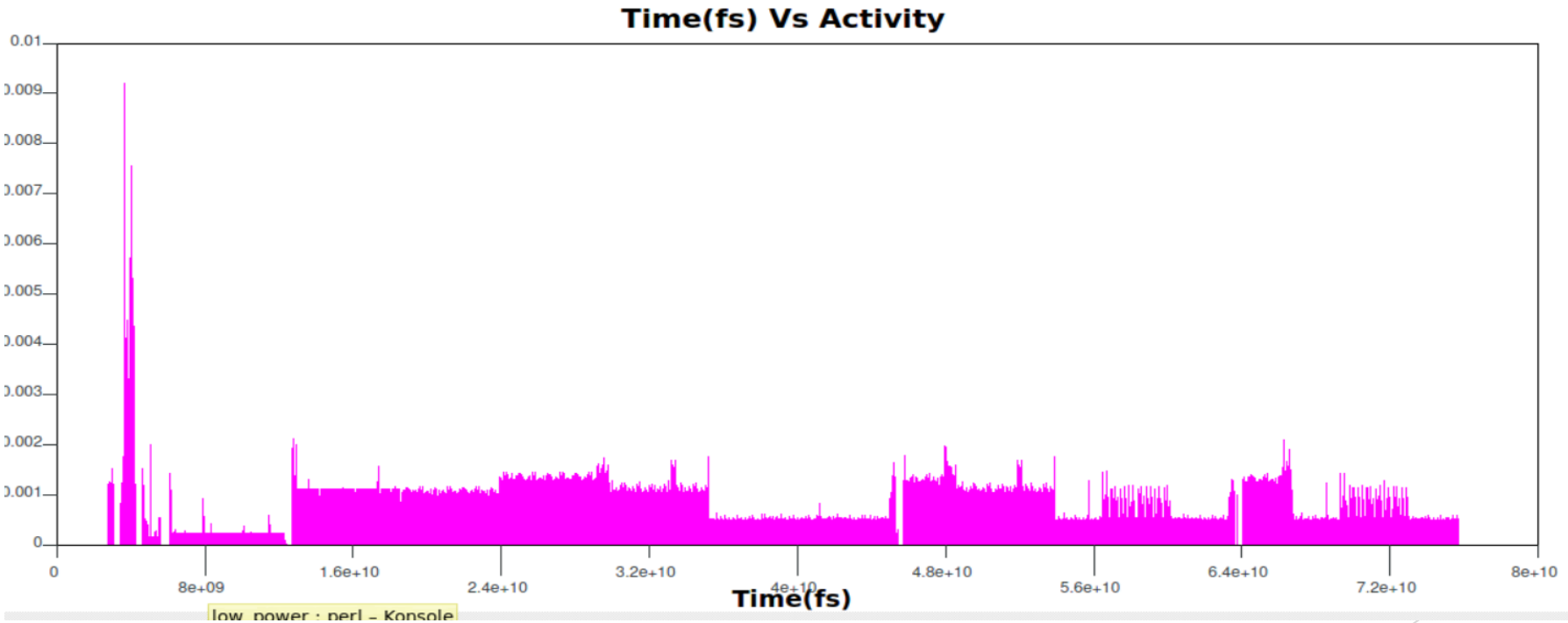


Power Reduction Methodology



Power Reduction Methodology: Activity

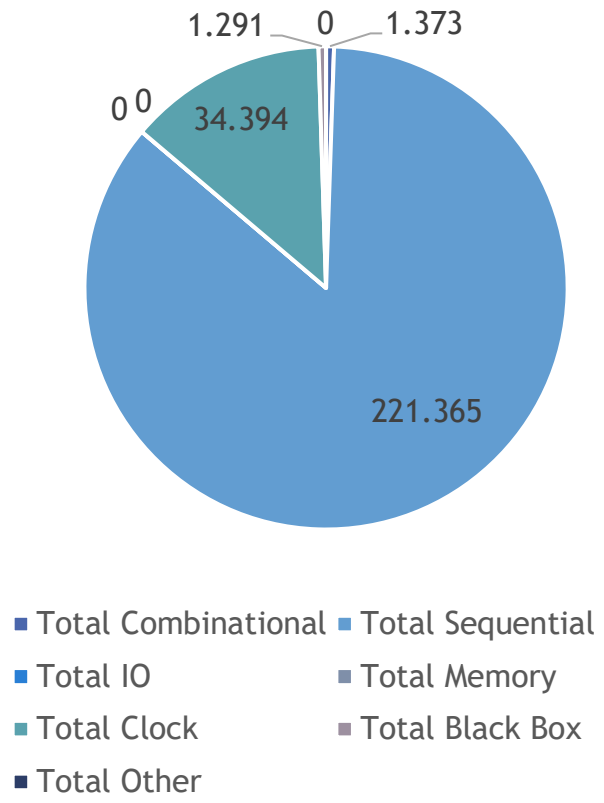
Time versus Activity filters out crucial time stamps, allowing for more accurate power analysis. The given figure aids in selecting suitable intervals for power analysis and ensures that the test benches have adequate functional coverage.



Power Reduction Hierarchies

▶The design information of all underlying hierarchies is analyzed. The proposed design attributes for early-stage power exploration are:

- Design/Block Status
- Annotation Status
- Clock Gating Status
- Register Gating Status
- Gating type



Power distribution across different logic blocks

Power Reduction Hierarchies (Contd.)

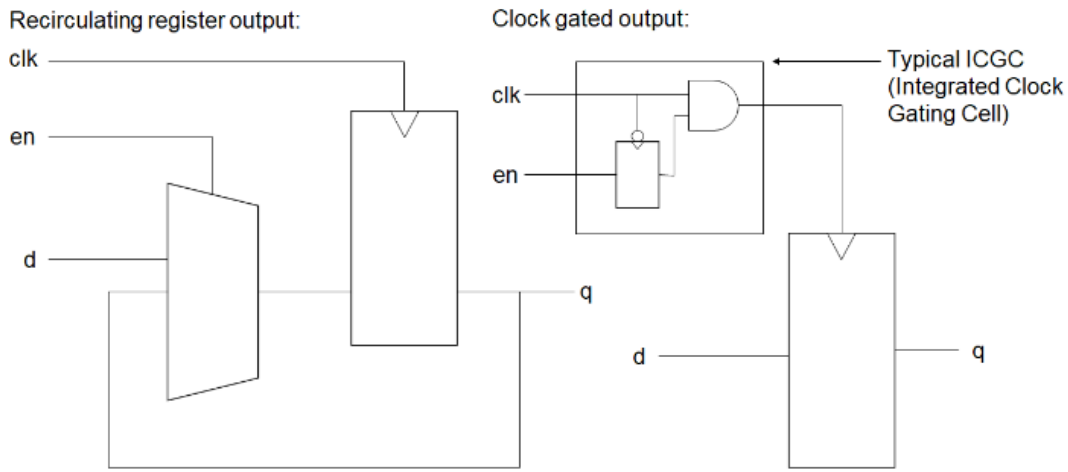
- Clock gating regression was done to identify gating opportunities across multiple simulation files.
- Hierarchies with poor clock gating, poorly gated registers, and memories were identified. Few of the parameters are stated in the following figure.

Instance Heirarchy	Average Register D Pin Activity	Average Activity	Average Clock Pin Activity	Average Driving Clock Activity	Average Clock Gating Efficiency (%)	Average ROADF(%)	Average ROADE(%)	Average QD(%)
local_logic	0.015	0.015	0.415	1.100	68.655	6.613	21.672	74.398
local_logic_1	0.000	0.015	0.175	0.507	65.546	0.000	4.878	NA
local_logic_2	0.049	0.034	0.714	0.985	53.333	13.469	38.159	63.618
local_logic_3	0.049	0.033	0.714	0.985	53.333	15.201	41.206	68.633
local_logic_4	0.036	0.017	0.714	0.985	53.333	3.628	6.667	94.521
local_logic_5	0.051	0.031	0.714	0.985	53.333	13.85	27.492	62.647
local_logic_6	0.029	0.019	0.571	0.854	55.814	2.965	25.581	97.203
local_logic_7	0.029	0.019	0.571	0.854	55.814	2.965	25.581	97.203
local_logic_8	0.016	0.022	0.857	2.000	57.143	3.829	3.829	100.000
local_logic_9	0.015	0.021	0.857	2.000	57.143	3.604	3.604	100.000
local_logic_10	0.000	4.26E-03	0.857	2.000	57.143	0.000	0.000	NA
local_logic_11	0.013	0.018	0.857	2.000	57.143	2.928	2.928	100.000
local_logic_12	NA	0.000	NA	NA	NA	NA	NA	NA
local_logic_13	0.000	0.013	0.516	0.532	11.111	0.000	0.000	NA
local_logic_14	NA	0.000	NA	NA	NA	NA	NA	NA
local_logic_15	0.000	0.000	0.000	0.247	100	NA	NA	NA

Hierarchical based matrix to investigate power loopholes

Enable and Clock Gating

- The proposed methodology is to use an integrated clock-gating cell (ICGC). This is advantageous for designers as the power consumed by this ICGC is generally much less than the conventional re-circulating register.
- This ensures better enable and clock gating.



Mix Voltage Thresholds (Vt)

Multiple Vt levels have been used to minimize active leakage power and delays.

The library contains two or more cells with the same function, same operating voltage, different cell names, and different leakage values in this design. One variation of the cell (low Vt) is faster but has more leakage, while another variant (high Vt) is slower but has less leakage. The designer's motivation is to minimize leakage while still achieving the timing estimates.

Power Register Reduction

The other advanced methodology is to reduce the power of the register part of the design. The vital data observed here is the Q/CP ratio, where Q denotes the output frequency and CP denotes the clock frequency. It is also termed Register Output Activity Density per Flip-flop (ROADF). This helps identify registers for which the data is not toggling, but the clock pin is toggling.

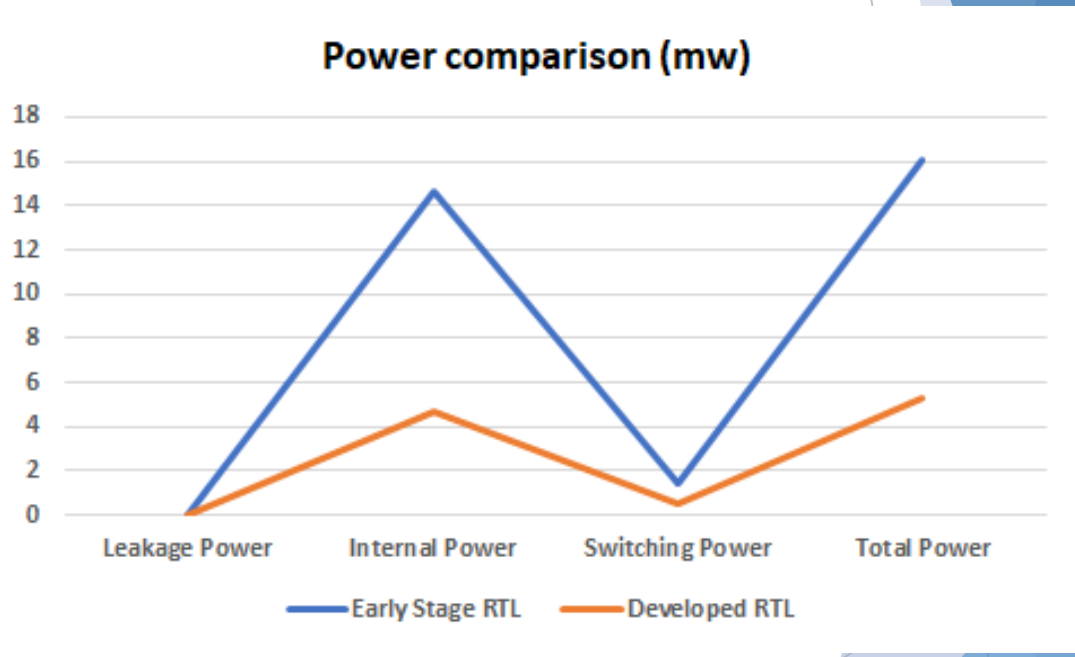
This is also a power bug. Low Q/CP marks the need to determine a new enable or strengthen the enable of the given register.

Research Elaborations

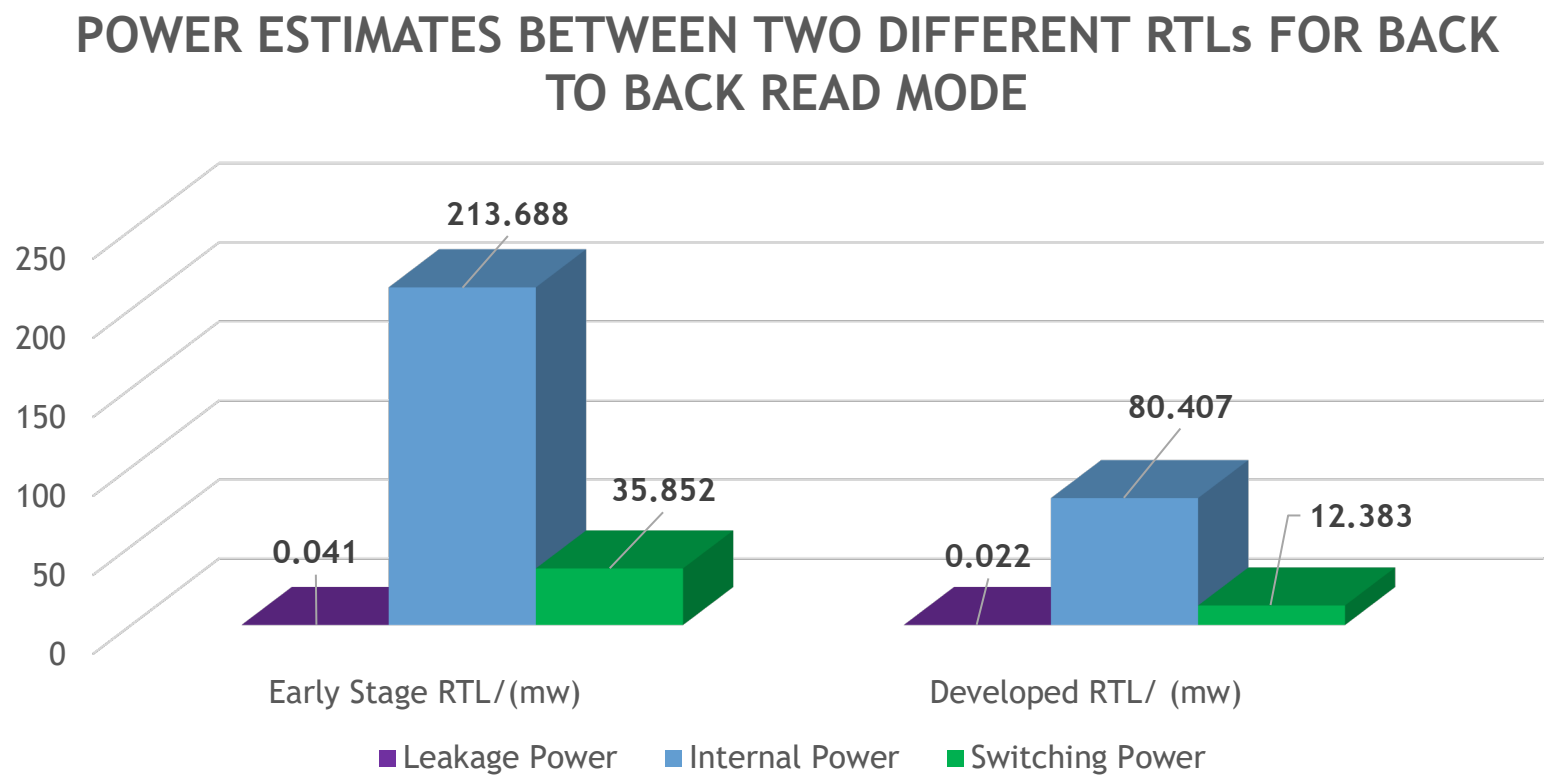
- Considering the scenarios when PHY does normal functions such as reading, writing, and routine updates.
- It is ludicrous to think that consumption should be the same in all conditions.
- Therefore, it is critical to understand the importance of dynamic and static power in all these scenarios.
- Power flow exploration using two RTLs: an ongoing RTL that has yet to release the netlist and a stable RTL with a finalized netlist and structure. The two RTLs taken have almost similar functionalities and structures for comparison.
- The first design is a functional design that will be improved in the future. The second design has a more enhanced, pipelined, and unvarying flow. The development cycle becomes crystal clear by comparing the outcomes of the ongoing design to the stable design. Designers will get the power numbers to compare and analyse the design's power requirements. As a result, any major or minor changes can be made considering power numbers.

Results

- The power numbers presented are from thorough verification in all possible operational modes simulated at TSMC 5nm technology node.
- Power estimation, exploration and reduction have been performed on several subcategories.
- Different categories are considered for low power design, including memories, latches, I/O pads, flops, clocks, and other sub-sections.



Results (Contd.)



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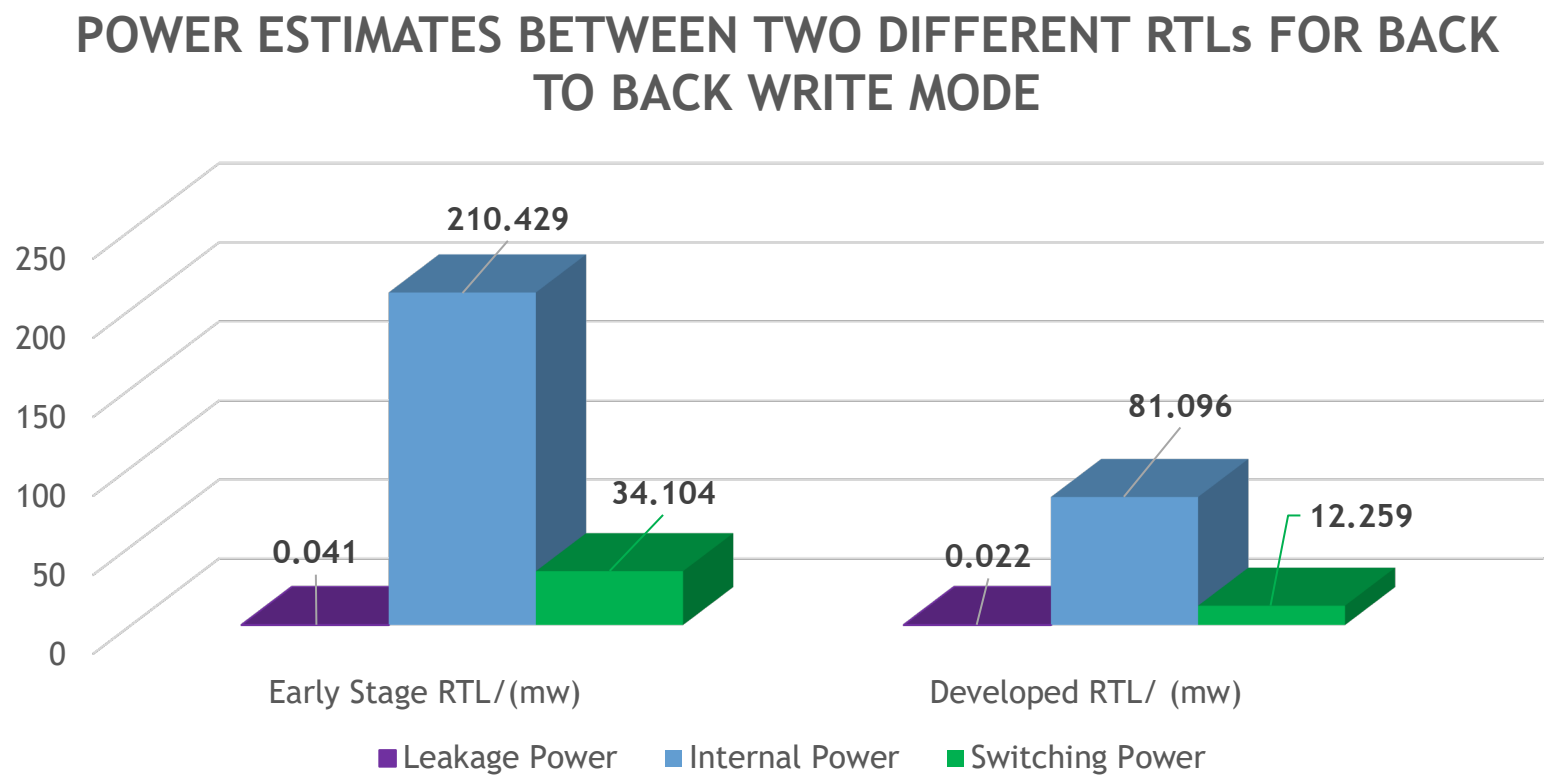

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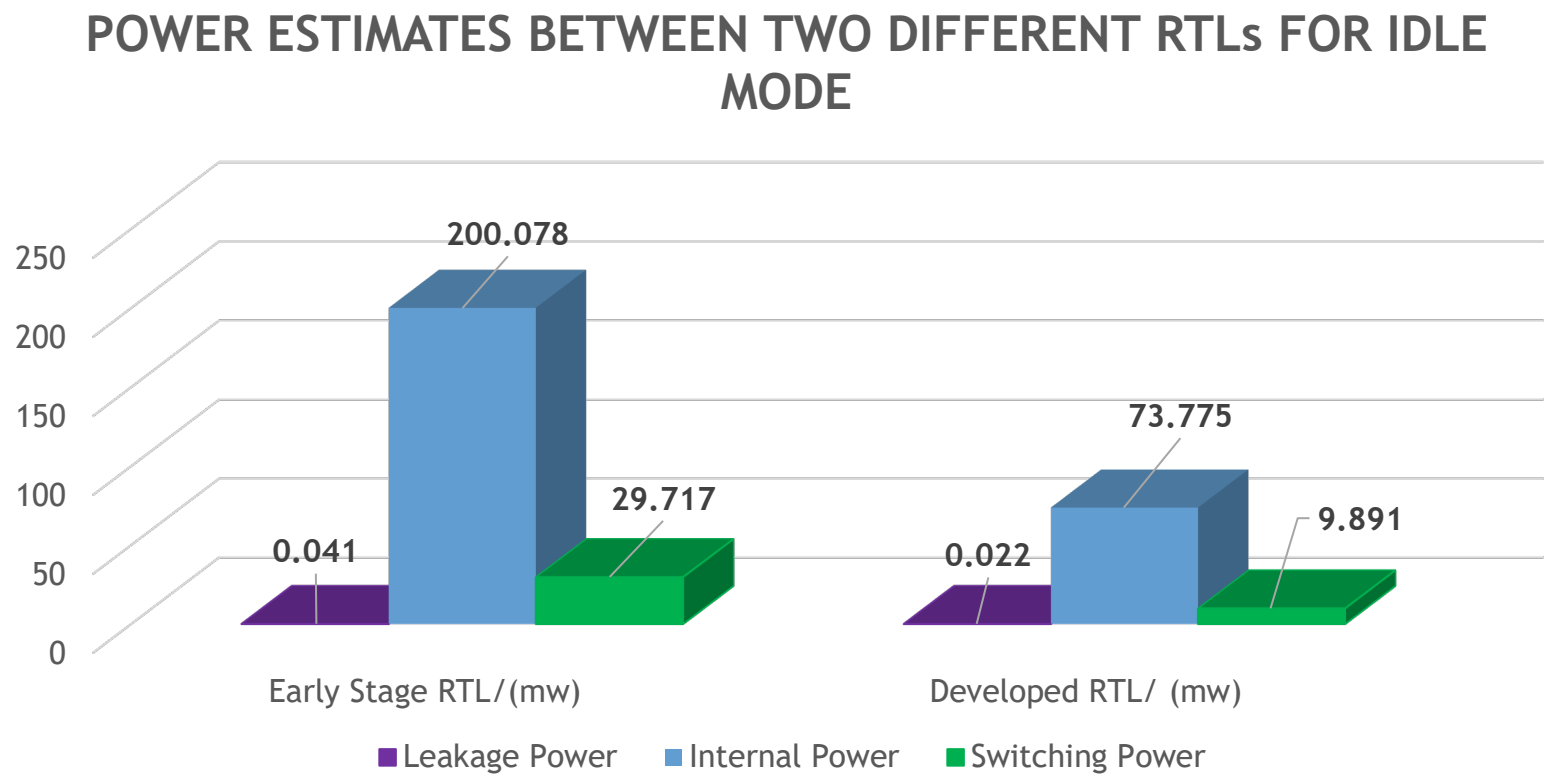

Conclusions

- This work presents a comprehensive method that addresses all elements of power analysis, including early RTL estimate and exploration, by using the RTL Spyglass signoff tool.
- This delivers meaningful feedback regarding the design architecture from a low power perspective at the RTL stage in a user-friendly manner.
- This process can be standardized and included as an add-on feature in simulators by verification teams.
- This methodology allows design teams to create the Spyglass Power log file for each accompanying RTL module.

Thank you