A Novel Simulation Flow for 7nm Mixed-Signal Design Transistor Level Verification

Pei Yao, Lei Zhou, Stanley Chen, Peter Chen
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Agenda

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2. Xilinx/AMD Traditional AMS Simulation Flow and Issues
3. New AMS Simulation Flow
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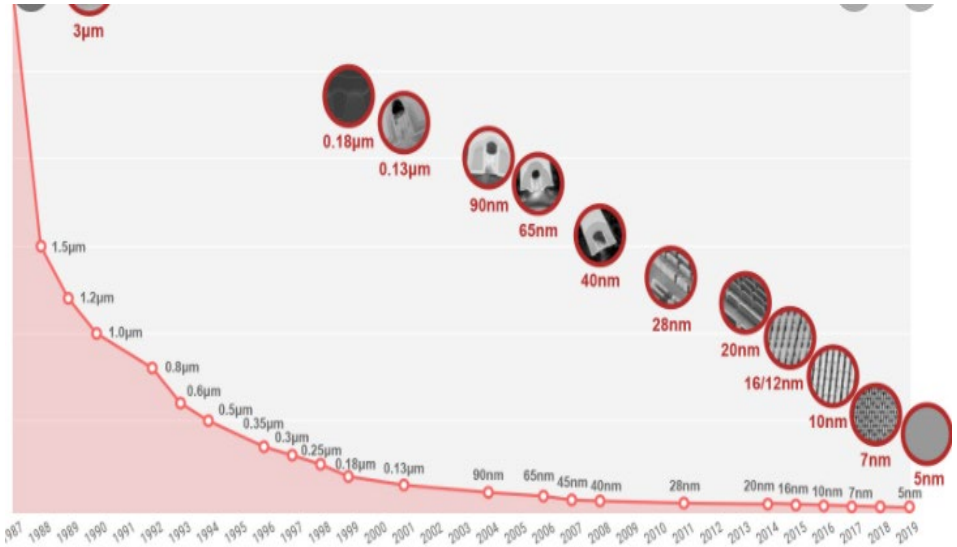
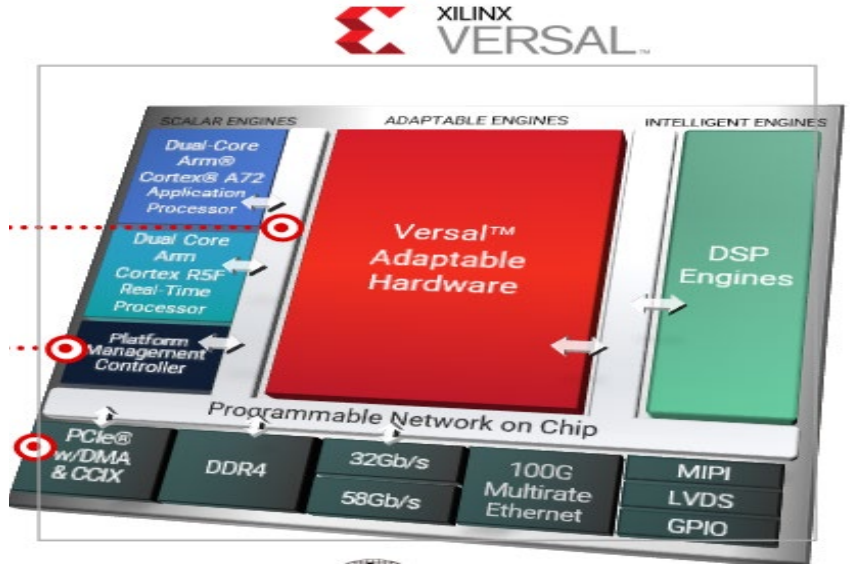
5. Summary

7nm AMS Simulation Challenges

- Process technology continue to scale down
  - Advanced and complicated device models are required
  - Number of parasitic components increases
- More complexed chip
  - More function blocks integrated
  - Tighter design margins
  - Increased demand for design coverage
- AMS Simulation Flow Challenges
  - Longer turn around time
  - Requires larger simulator capacity
  - Demands more computation resources





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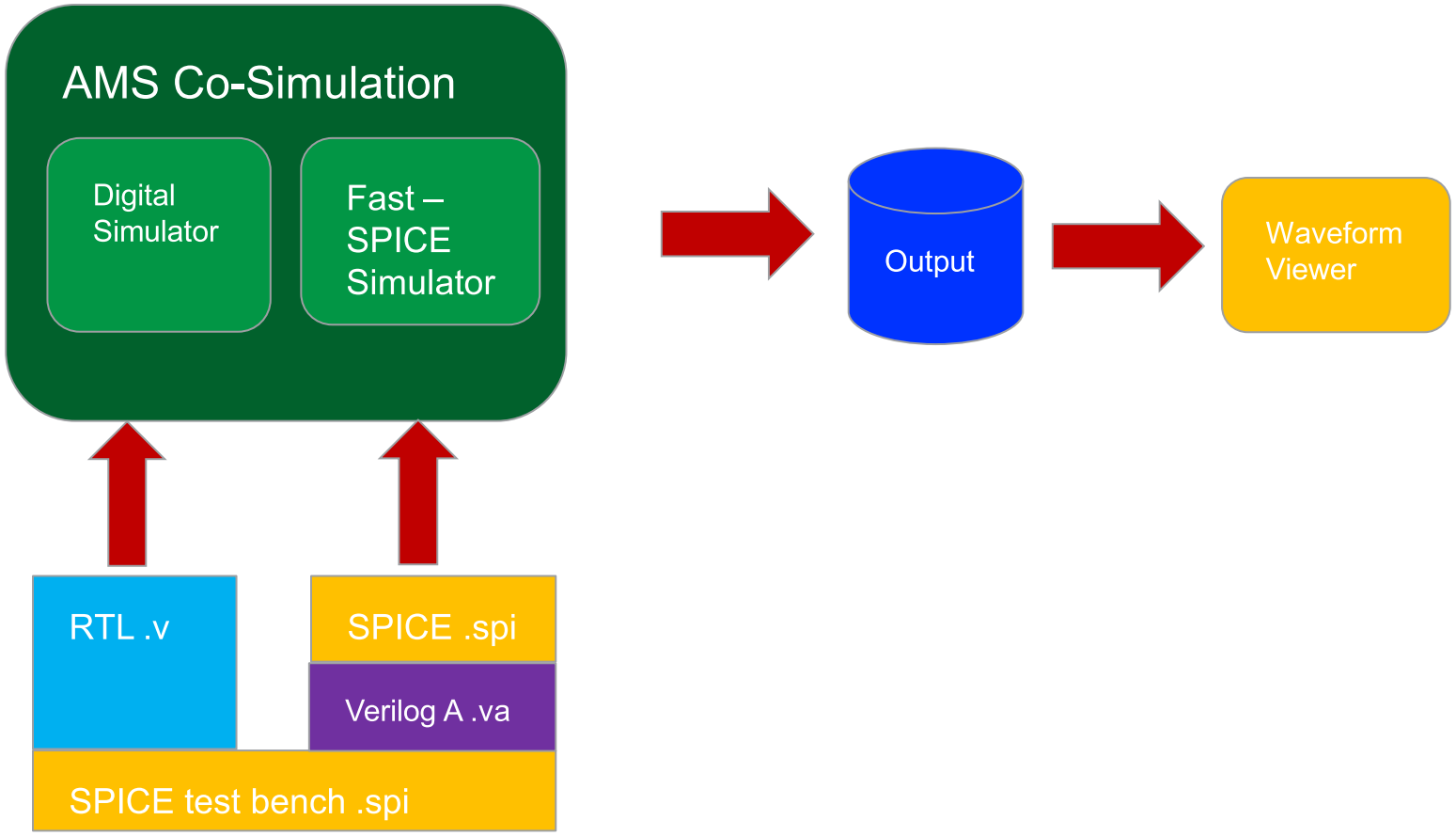
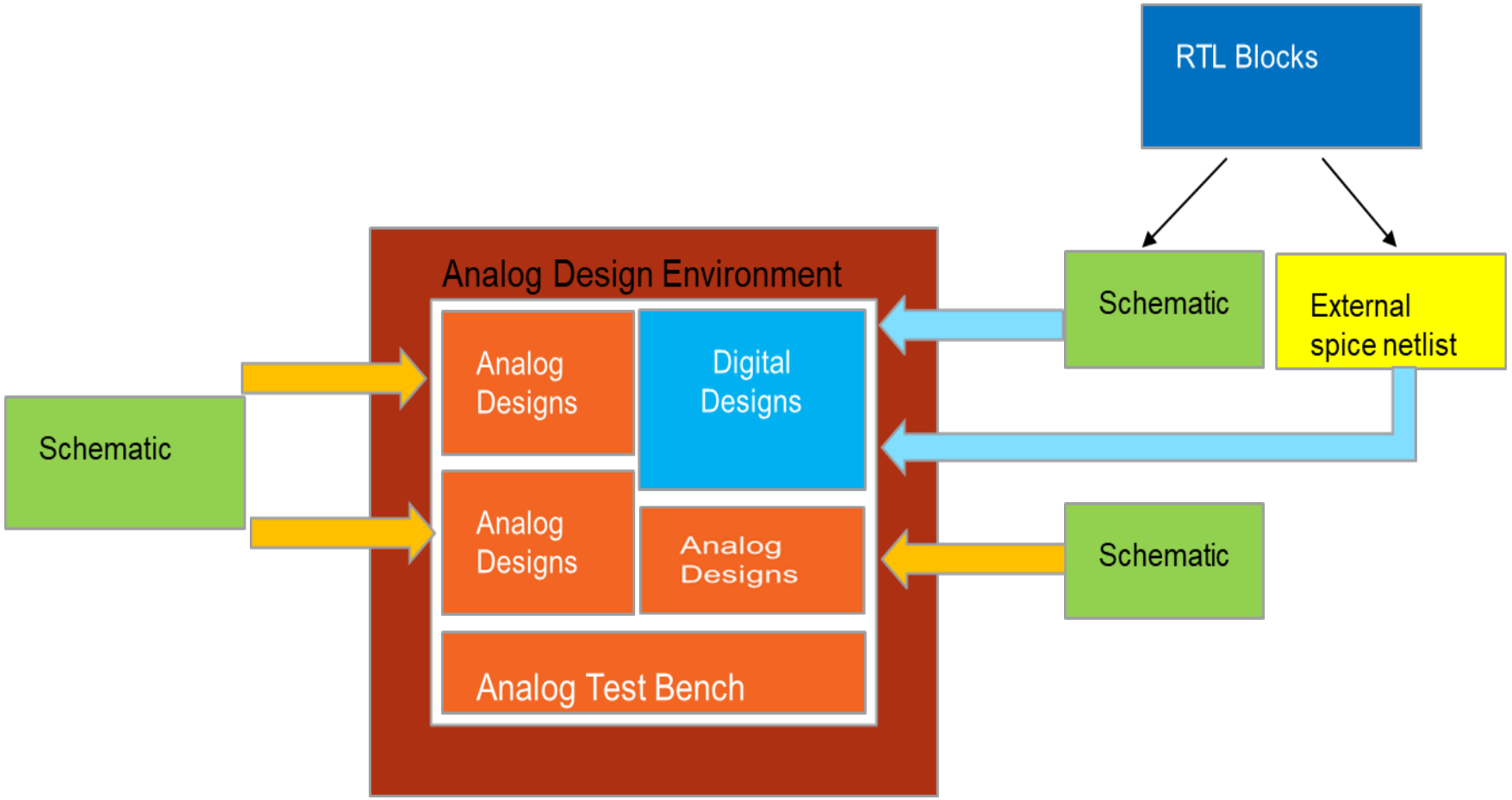
Xilinx/AMD Traditional AMS Simulation Flow and Issues



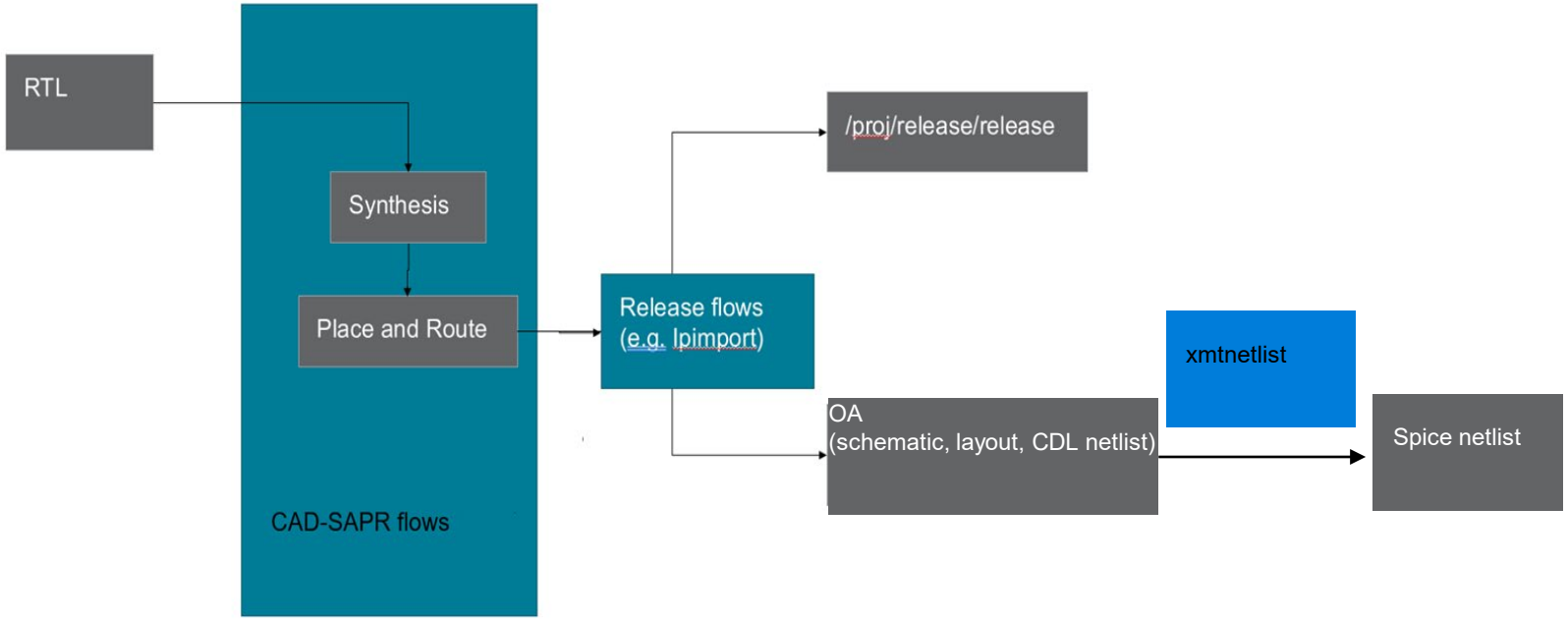
- Fast SPICE simulator can't achieve high accuracy required for high frequency components
- Switch between the command line-based environment for mixed-signal verification and the schematic based analog design environment.
- Need a new solution to speed up simulations time while maintaining good accuracy

New AMS Simulation Flow with RTL Blocks



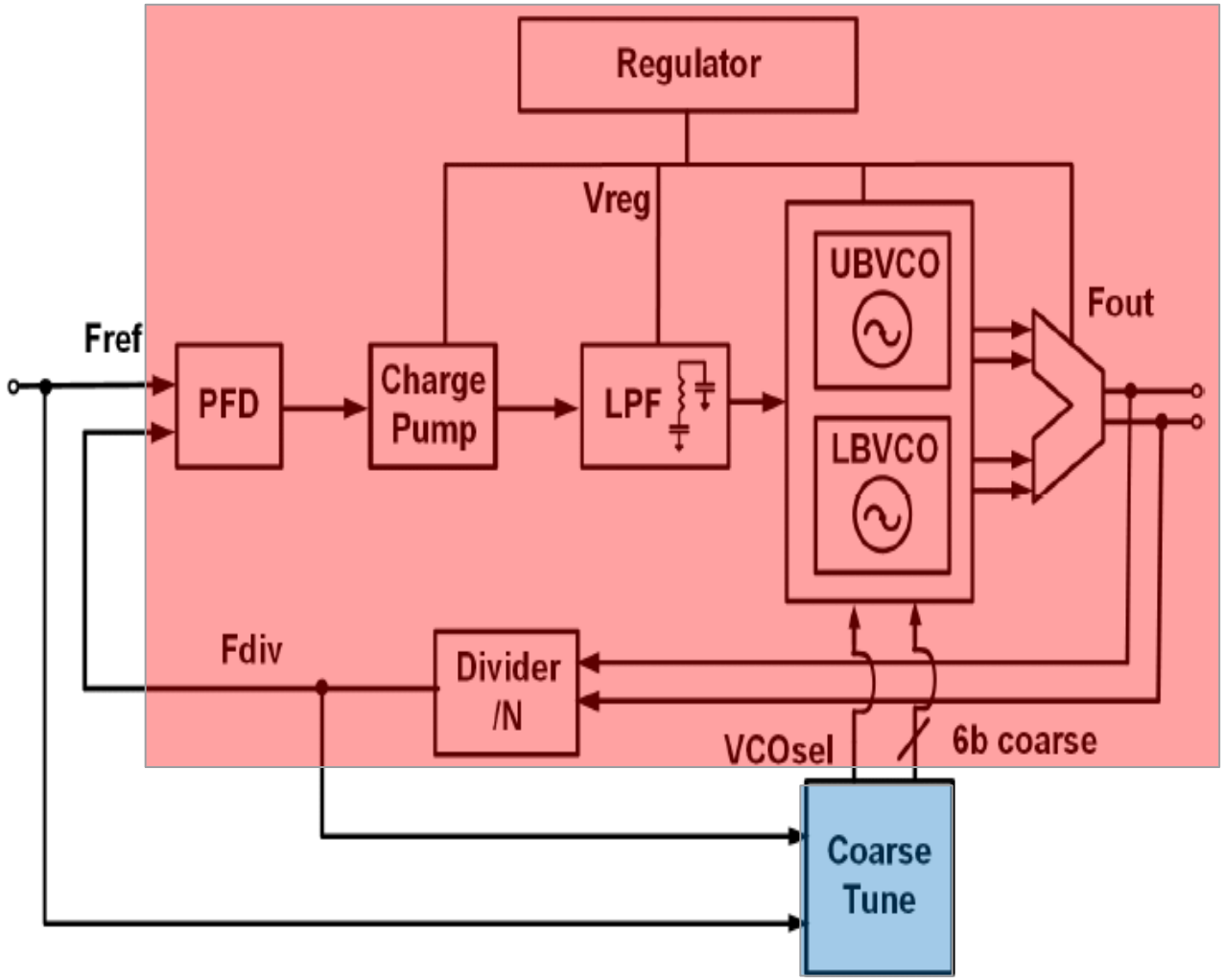
- Single environment for analog simulation and mixed-signal verification.
- Digital RTL is imported into schematic or an external SPICE file.
- High performance analog SPICE simulator is used to simulate both digital and analog blocks and deliver faster performance and better accuracy.

Importing RTL using Xilinx/AMD Digital IP Release Flow



- Digital IP assembled from RTL in a Synthesis, Place & Route (P&R) flow
- P&R tool writes design definition in Verilog, DEF, LEF
- Industry utility converts Verilog to CDL.
- Run the internal IP-import flow to enable downstream consumption
  - Stub verilog (pins only) imported to OA as stub schematic view
  - LEF imported to OA as stub layout view
- Special flow xmtnetlist to trace the hierarchy and build a suitable netlist, which is fed into the high-performance analog SPICE simulator.

Case Study: LCPLL Block Diagram



Analog

Digital

- Most challenging case in transistor level simulation.
- Slow PLL loop convergence requires simulation of long circuit time in the order of µs.
- VCO requires fine time step in the ps range due to its high frequency

*D. Turker et al., “A 7.4-to-14GHz PLL with 54fsrms jitter in 16nm FinFET for integrated RF-data-converter SoCs,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, Feb. 2018, pp. 378–380.

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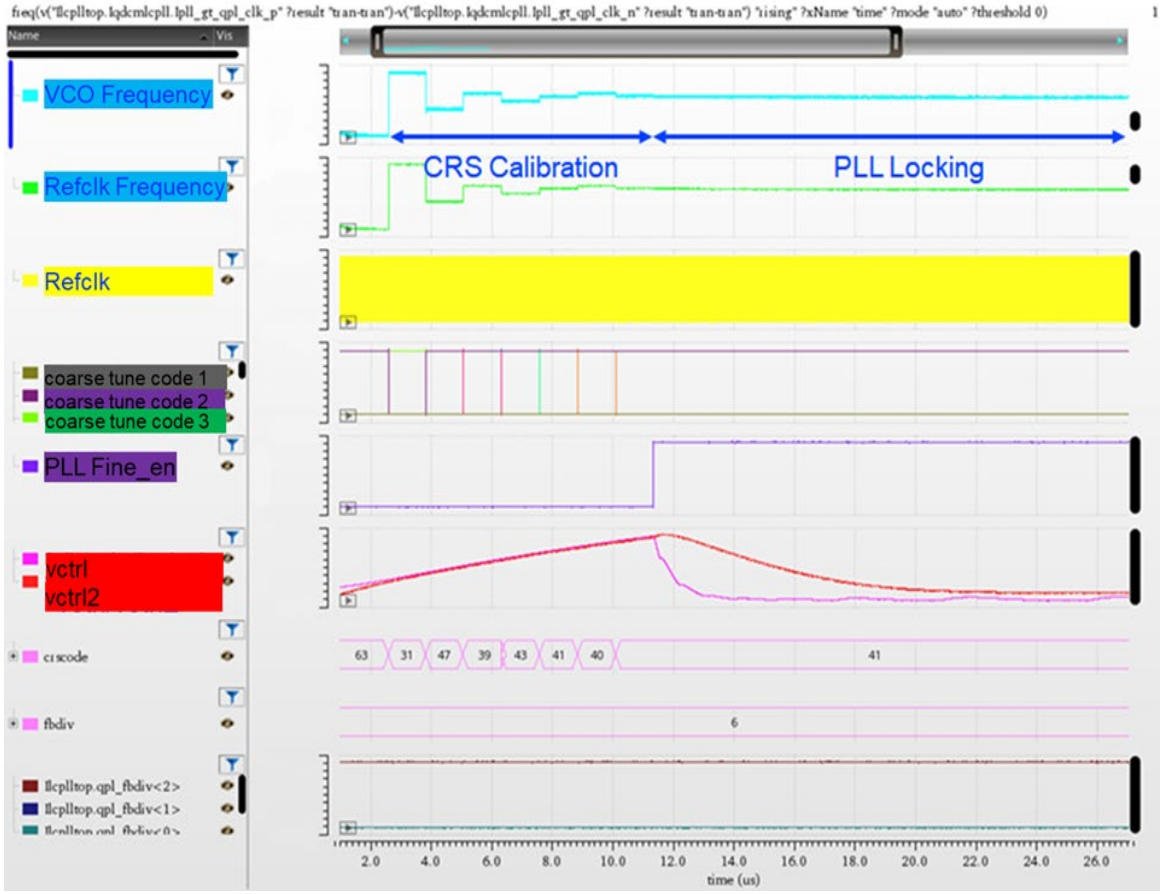
Flow Setup and Results:

- Digital RTL code is imported into schematic and netlisted together with analog blocks.
- Top level test bench is imported from analog testbenches with customizations.
  - Import register settings from csv file
  - Optimize power up/down and reset sequence to speed up simulation
- Run simulation with parallel analog SPICE simulator in VX mode.
- Simulation results are verified using waveforms and measurement expressions.
- The simulation time is reduced from months to weeks, and the accuracy is sufficient for verification.

Simulation Results

- Circuit Inventory:
  - 1.28M Nodes, 334 K Transistors, 2.02M Capacitors, 1.0M Resistors.
- Simulation Time: 100µs
- Complete PLL simulation in 12 days from the initial coarse hunting phase to the fine vctrl set up phase
- The simulation captures different dynamics of the two phases
  - Phase 1:CRS Calibration
    - Coarse tuning of VCO frequency
    - Initial toggling of RTL code
    - vctrl1 and vcotrl2 ramp up
  - Phase 2: PLL Locking
    - VCO frequency converges to reference clock frequency
    - RTL code stabilize
    - vctrl1 and vctrl2 settle



Conclusion

- A novel AMS simulation flow is presented using parallel analog SPICE simulator for mixed-signal functional verification for 7nm designs.
- Both block level simulation and top-level functional verification can be performed in the same environment, eliminating the need of switching design flows.
- This flow is proven efficient to detect potential bugs at early design phase. It reduces design cycle and provides confidence for final sign-off.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