Role of Memory in Future Compute Architectures
A Story of Technology Disruption

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Forward-looking Statements

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Semiconductor Industry at a Glance

Memory
(DRAM, NAND, Emerging & others)

28%

Source: Gartner - Semiconductor Market Share Report, 2020-2021
Semiconductor Industry at a Glance

2021

- Memory (DRAM, NAND, Emerging & others) - 28%
- Application specific (RF wireless connectivity, power management & others)

2030 Forecast

- Memory (DRAM, NAND, Emerging & others) - 34%
- Application specific (RF wireless connectivity, power management & others)

Source: Gartner - Semiconductor Market Share Report, 2020-2021

Source: WD Forecast from Gartner – Semiconductor Market Share Report, 2020-2026
Moore’s Law: Wave that propels our industry
2000s – Disrupting Flash Memory

$150 in 2001

10x better

Source: TechTarget [25 Mar 2020]
No Exponential Lasts Forever
2010s – Disrupting Flash Memory…Again
Long Live NAND

Log [TB/Wafer]

Time

2016

2032

500+L

400+L

300+L

200+L

162L

112L

96L

64L
Moore's Law Slowing for Logic
Moore’s Law Slowing for Logic

Scaling continues through advanced packaging
Moore’s Law Slowing for Logic

Scaling continues through advanced packaging

Source: OCP Global Summit: "Software Defined Memory: A Meta Perspective"
**DRAM NOTaling**

- Moore’s Law
- Avg. DRAM Density Shipped
  - 1979-2003: 51% CAGR
  - 2003-2011: 29% CAGR

**DRAM Density Gap is Increasing**

- 1TB
- 512Gb
- 256Gb
- 128Gb
- 64Gb
- 32Gb
- 16Gb
- 8Gb
- 4Gb
- 2Gb
- 1Gb
- 512Mb
- 256Mb


- 8Gb – 15 years behind Moore’s law
- 4Gb – 12 years behind
- 2Gb – 8 years behind
- 1Gb – 5 years behind
- 512Mb – 3.5 years behind
- 256Mb – 3 years behind Moore’s law

Source: Quantifying the Performance Impact of Memory Latency and Bandwidth for Big Data Workloads, Russell.M.Clapp et al, 2015 IEEE International Symposium
**Memory Wall**

**Increasing Core Counts Drives Growth**

- Increasing core counts driving memory demand
  - Increased Bandwidth
  - Increased Capacity

**Increasing Memory Cost and Power**

- Memory an increasing % of system power and cost
  - Memory price (cost/bit) flat due to scaling challenges
  - Memory power scaling with speed

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Source: OCP Global Summit: "Software Defined Memory: A Meta Perspective"
2015s – Disrupting DRAM

- DRAM
- HOT
- 3D NAND
- WARM
- HDD
- COLD
2015s – Disrupting DRAM

- S/W ecosystem takes long time to build
- New silicon technology development exorbitantly expensive
- Large scale deployments require consistent performance
- Memory attach point critical to performance

Intel® Optane™ Persistent Memory
Solving Attach Point Problem: CXL

Direct Attached

- CPU
- DDR
- Native DRAM
- CXL
- CXL Memory Module

Memory Pooling and Sharing

- Computer Node
- CPU 0, CPU 1
- Memory Node
- M
- CXL Pooling Memory Controller
- CXL

Memory Centric Compute

- Memory + Fabric
- SoC
- Memory Fabric
- CPU
- Memory Node
- CPU 0, CPU 1
- DDR
Performance with CXL-Attached Memory

Performance slowdown under additional 64ns memory latency

One size does NOT fit all

Source: First-generation Memory Disaggregation for Cloud Platforms, Huaicheng Li et al, Mar 2022
Solving The Performance Problem

**S/W Driven**
- APP
- Native DRAM
- CXL Memory Module

**H/W Driven**
- Native DRAM
- CXL Memory Module
- IO Die

**M/W Driven**
- APP
- MIDDLEWARE
- Native DRAM
- CXL Memory Module

Logos:
- SAP HANA
- pmem.io
- Intel Xeon Scalable Processor
- VMware
- Meta
- Microsoft Azure
- MemVerge
Solving The Cost Problem

Conventional DRAM

Modified DRAM

New Memory Technology
Solving The Economics Problem

Incumbents  Venture Capital  Customers  Government
Where will the tide take us?
Western Digital
Create What’s Next
Performance with CXL-Attached Memory

Bandwidth demand vs latency sensitivity

Source: Quantifying the Performance Impact of Memory Latency and Bandwidth for Big Data Workloads, Russell.M.Clapp et al, 2015 IEEE International Symposium