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Role of Memory in Future Compute Architectures

A Story of Technology Disruption

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Forward-looking Statements

Safe Harbor | Disclaimers

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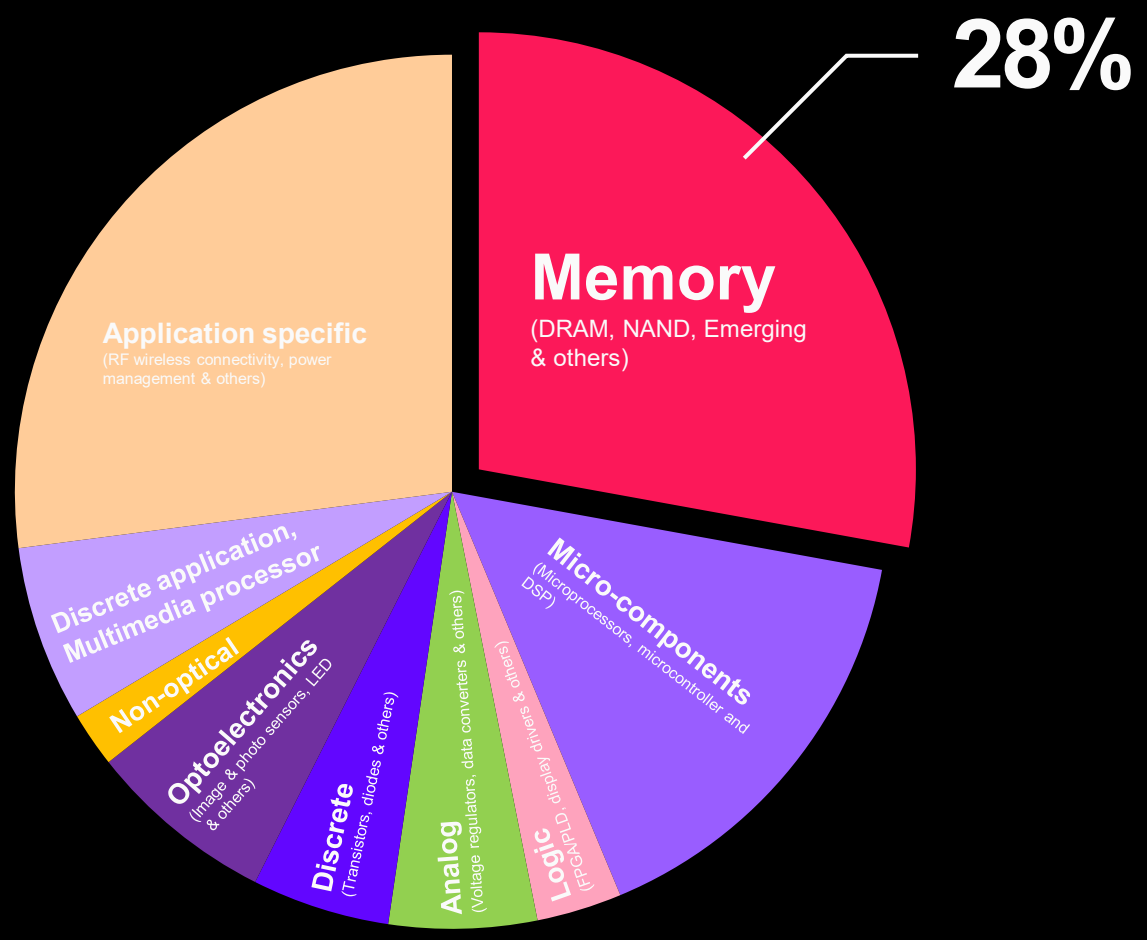
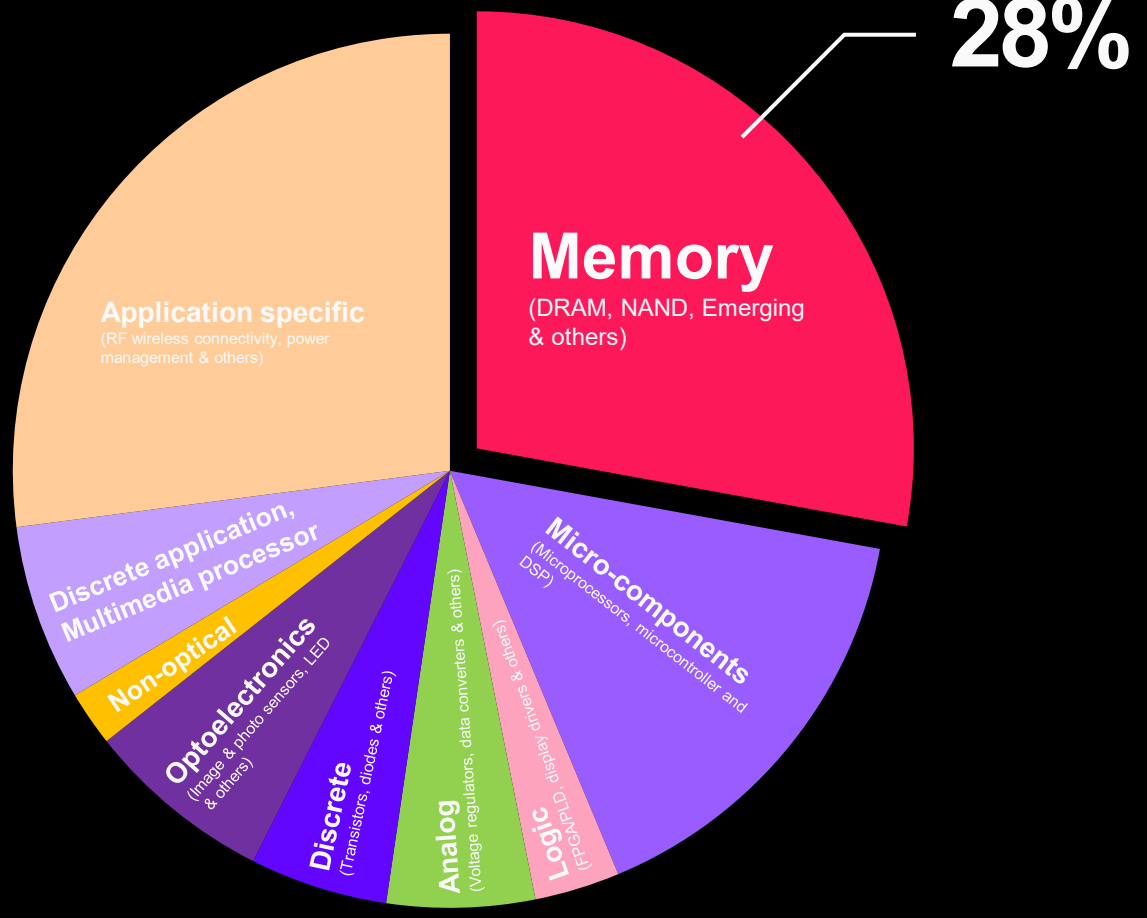
Semiconductor Industry at a Glance



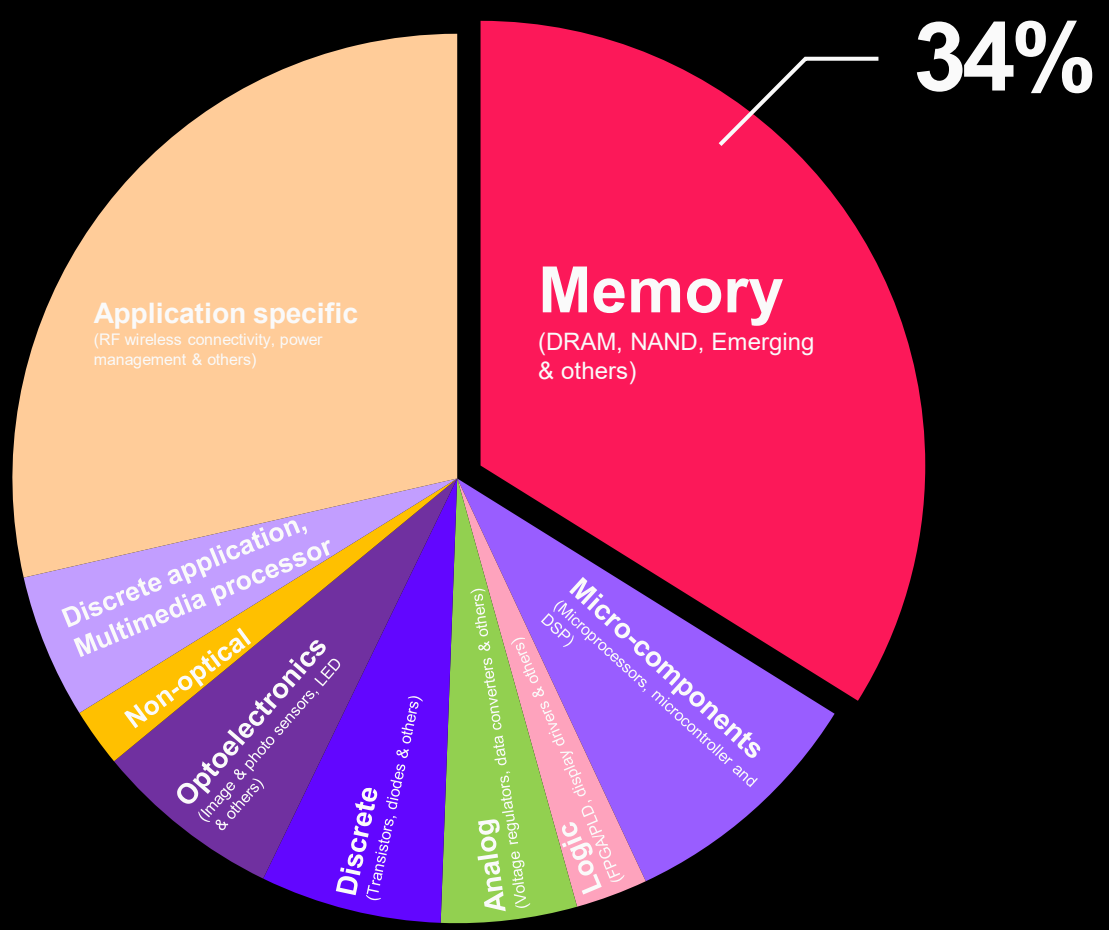
2021

Source: Gartner- Semiconductor Market Share Report, 2020-2021

Semiconductor Industry at a Glance



2021

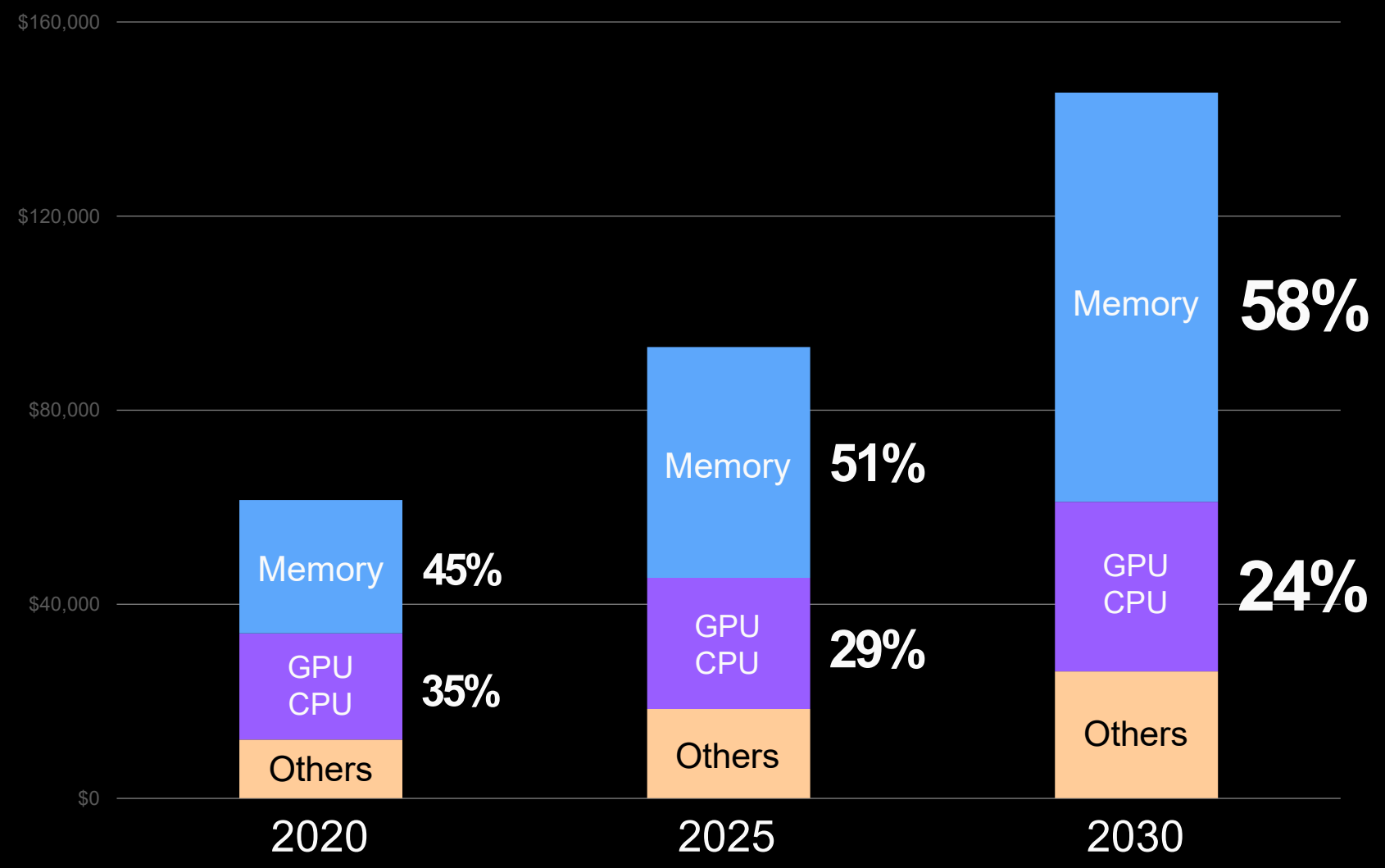


2030 Forecast

Source: Gartner- Semiconductor Market Share Report, 2020-2021

Source: WD Forecast from Gartner – Semiconductor Market Share Report, 2020-2026

Datacenter Semiconductor Revenues

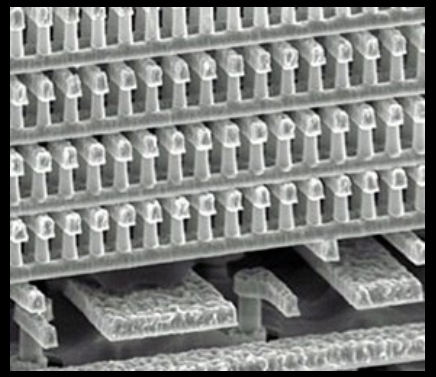


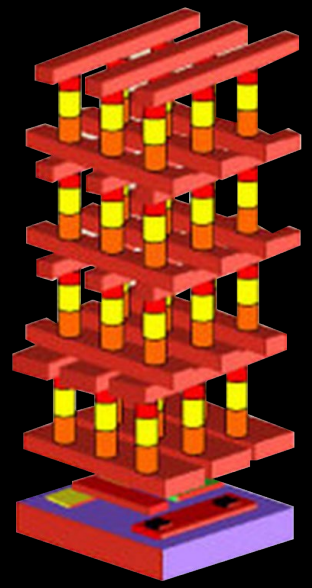
Source: Gartner- Semiconductor DC extract Forecast

Moore’s Law : Wave that propels our industry

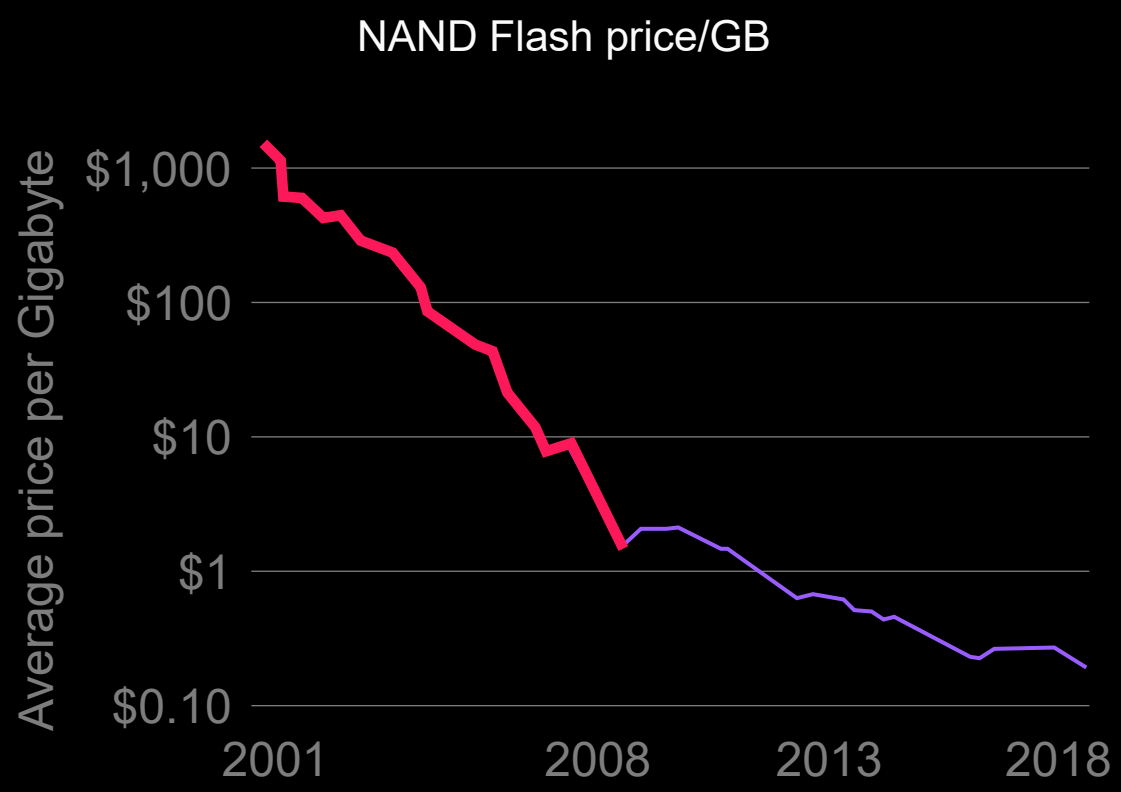
2000s – Disrupting Flash Memory

$150 in 2001





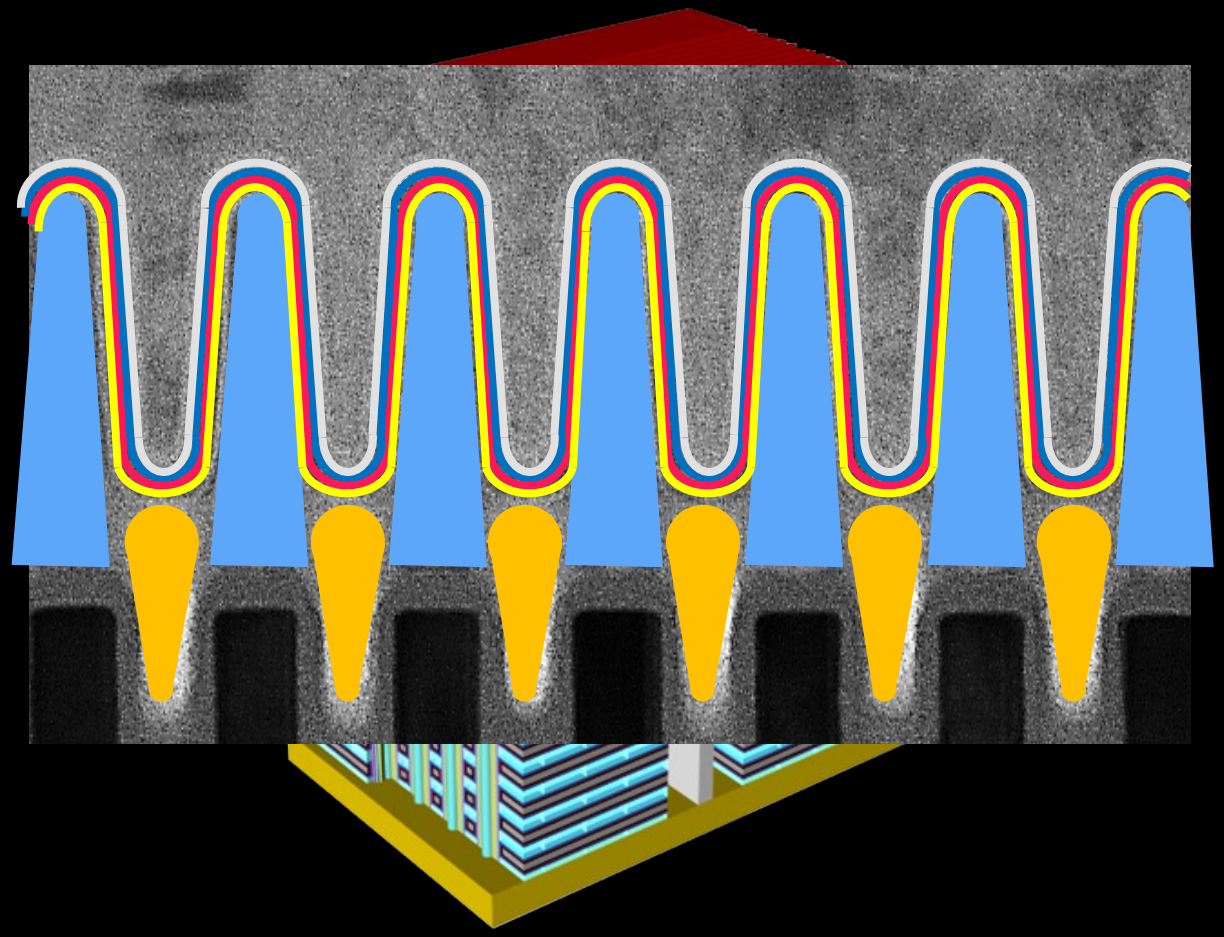
10x better



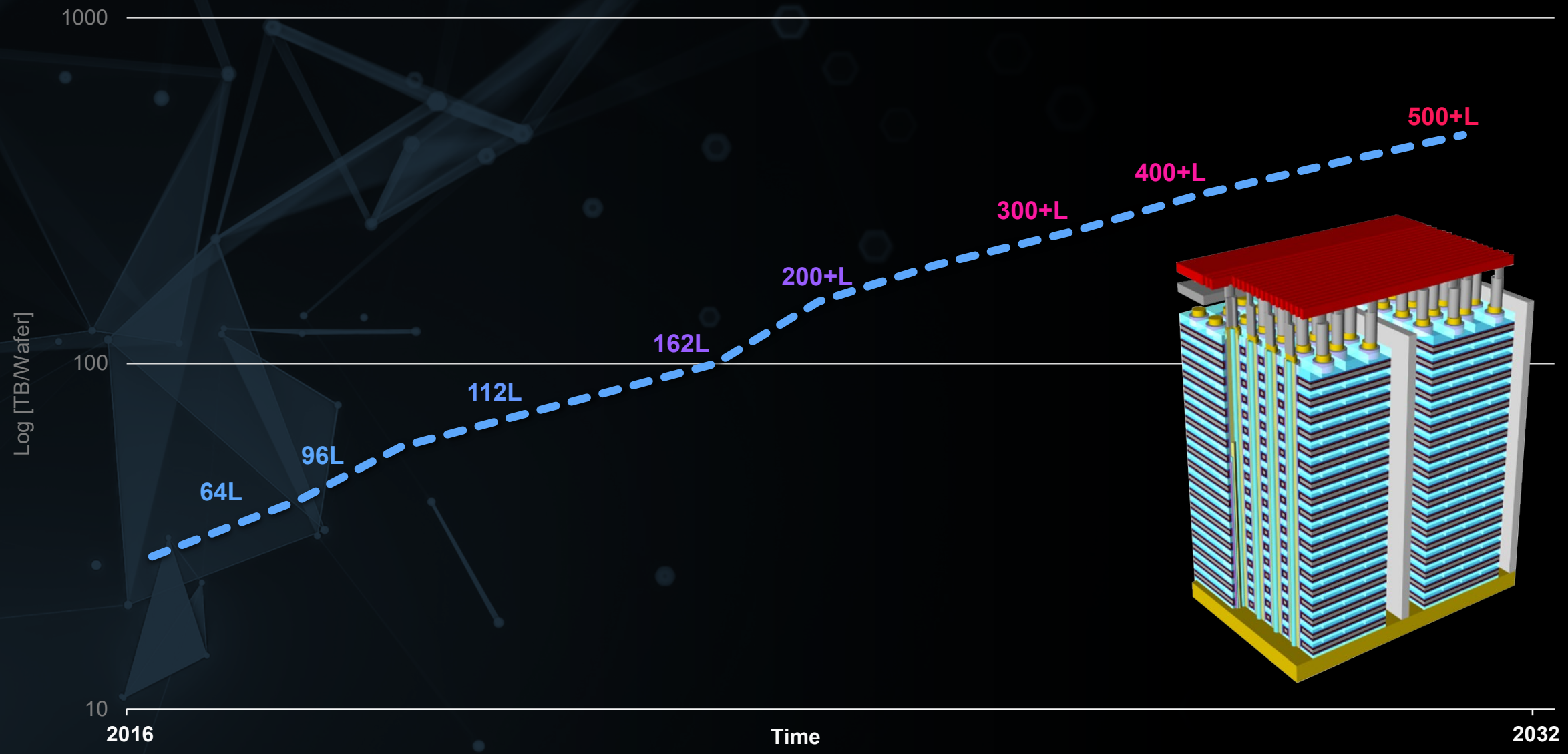
Source: TechTarget [25 Mar 2020]

No Exponential Lasts Forever

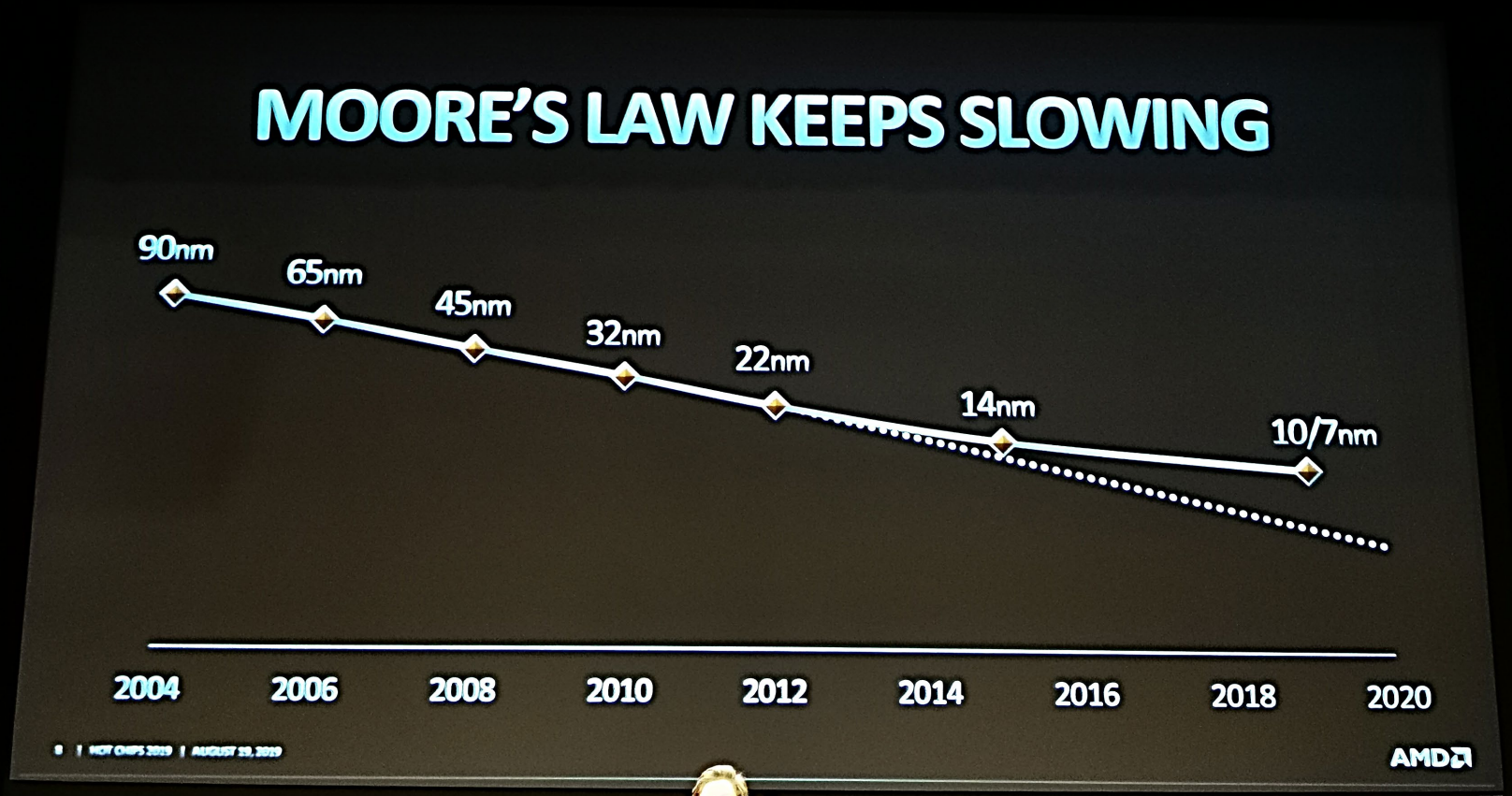
2010s – Disrupting Flash Memory…Again



Long Live NAND



Moore's Law Slowing for Logic



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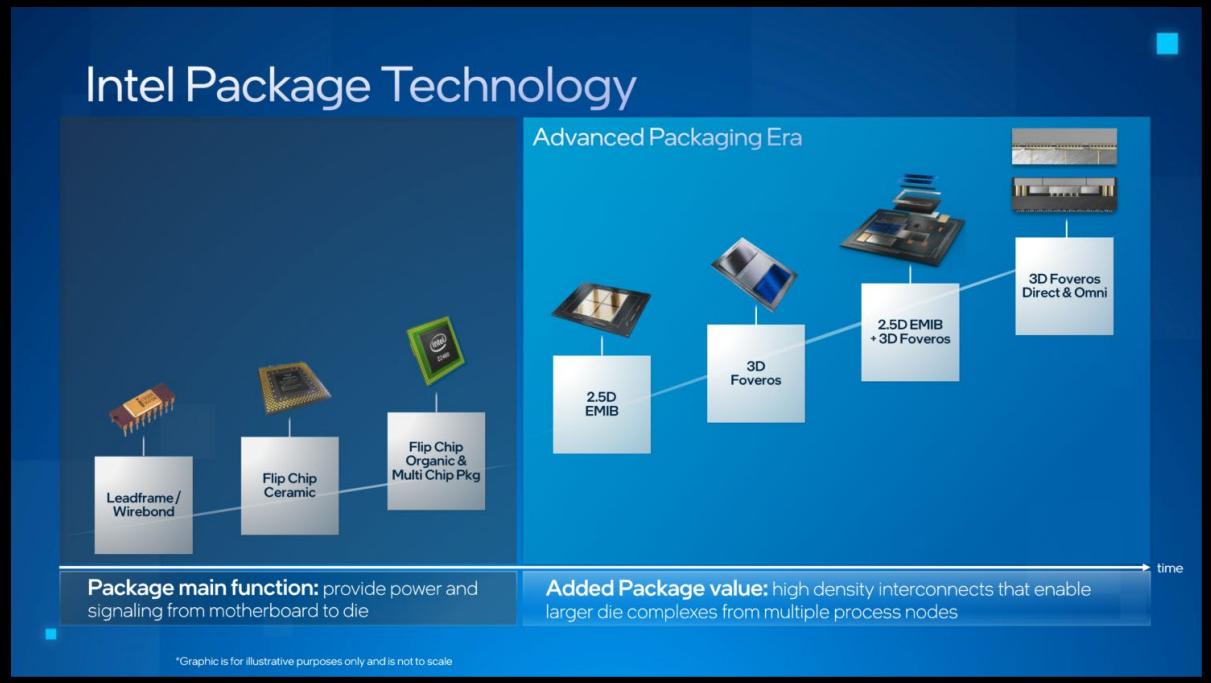
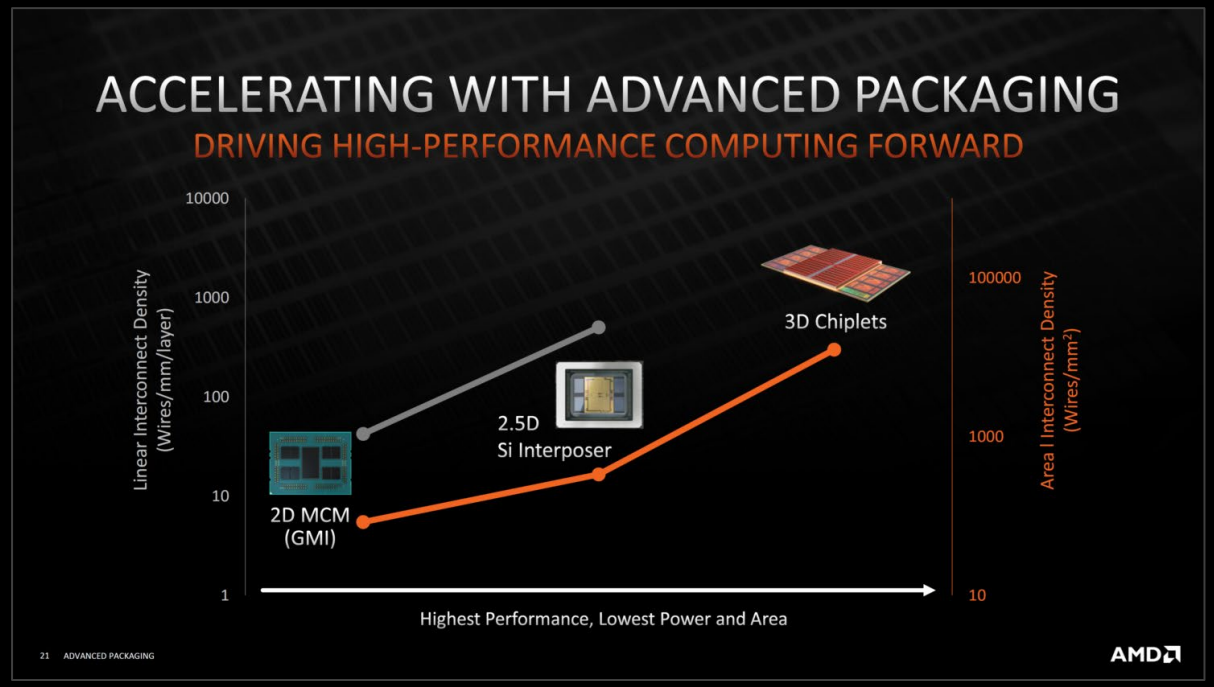
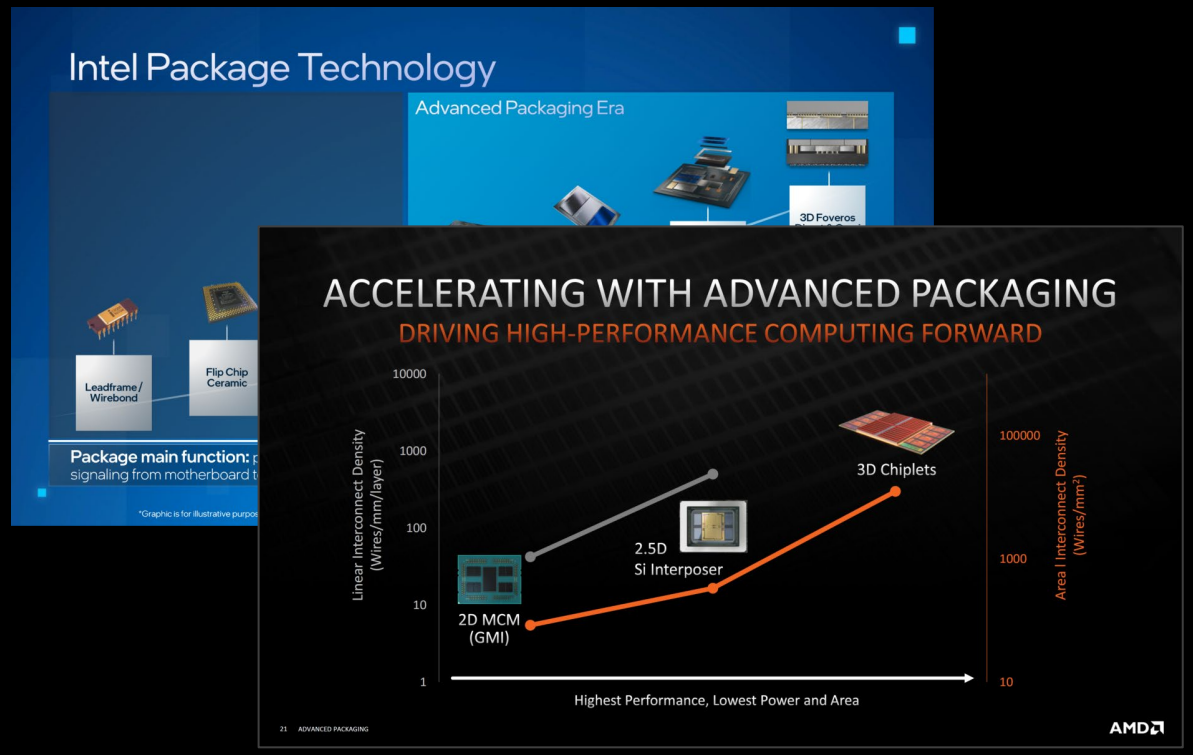
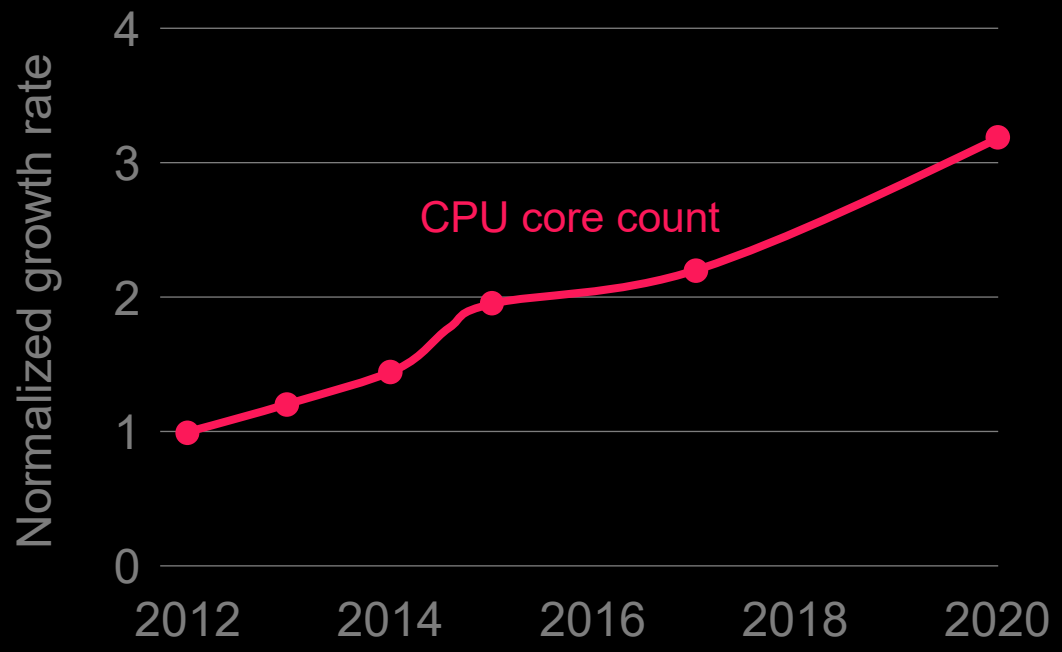




Scaling continues through advanced packaging

Moore's Law Slowing for Logic

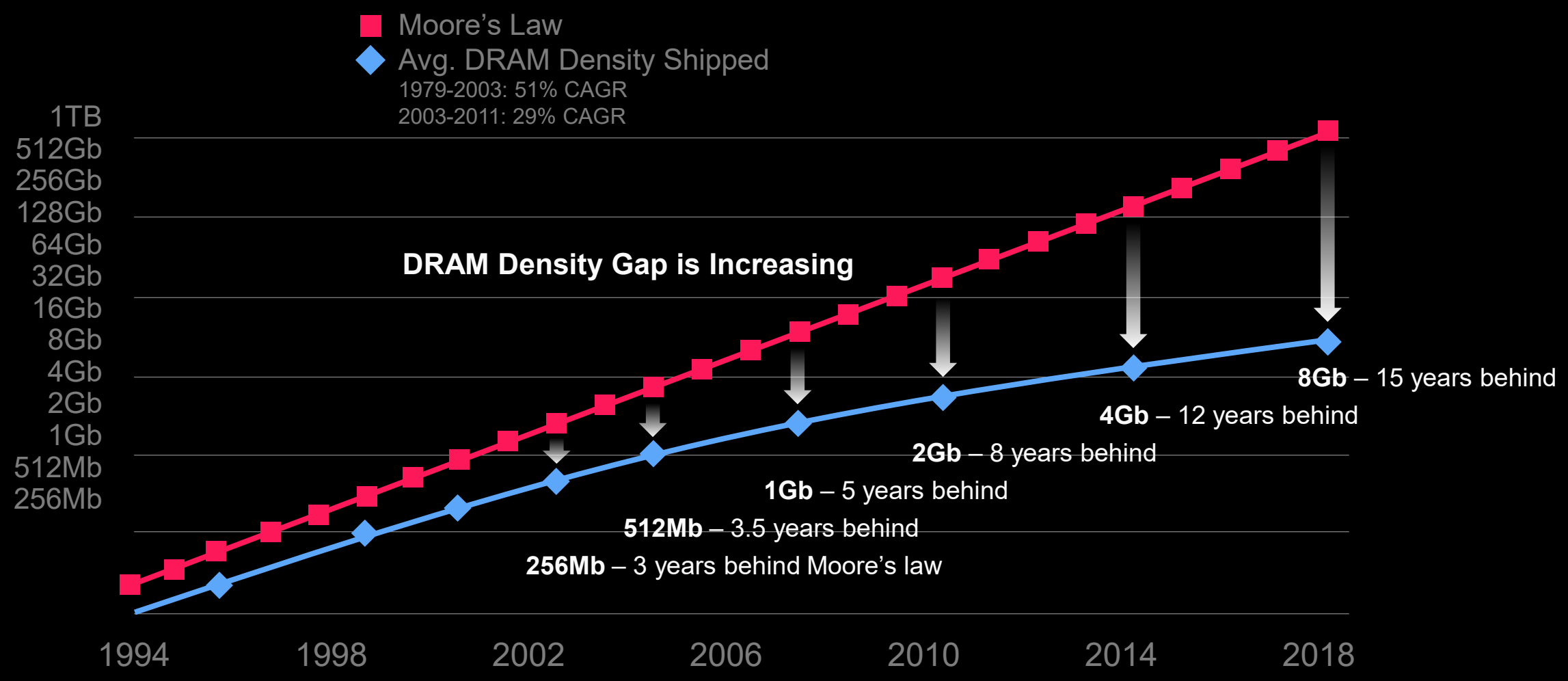




Scaling continues through advanced packaging

Source : OCP Global Summit : "Software Defined Memory : A Meta Perspective"

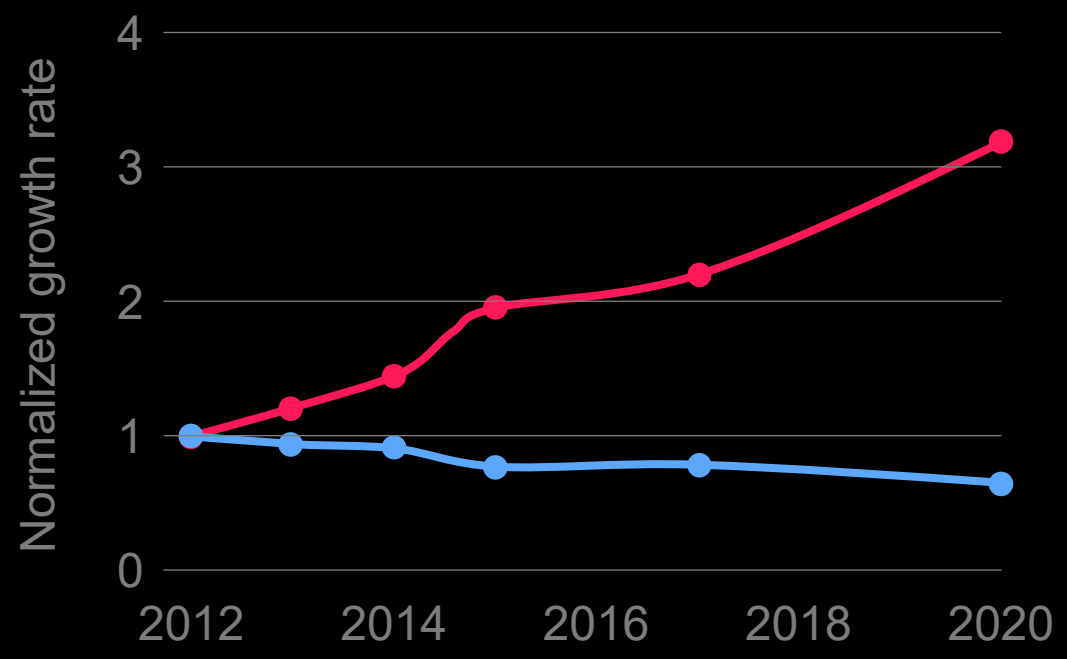
DRAI NOT aling



Source : Quantifying the Performance Impact of Memory Latency and Bandwidth for Big Data Workloads, Russell.M.Clapp et al, 2015 IEEE International Symposium

Memory Wall

Increasing Core Counts Drives Growth

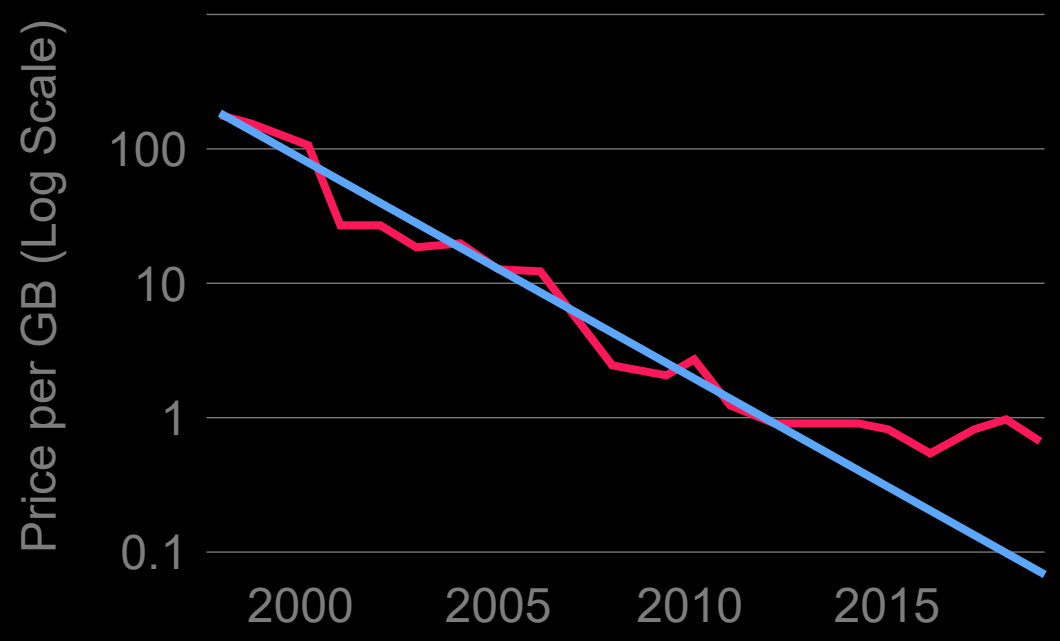


Increasing core counts driving memory demand

- Increased Bandwidth
- Increased Capacity

CPU core count Memory Channel BW per core

Increasing Memory Cost and Power



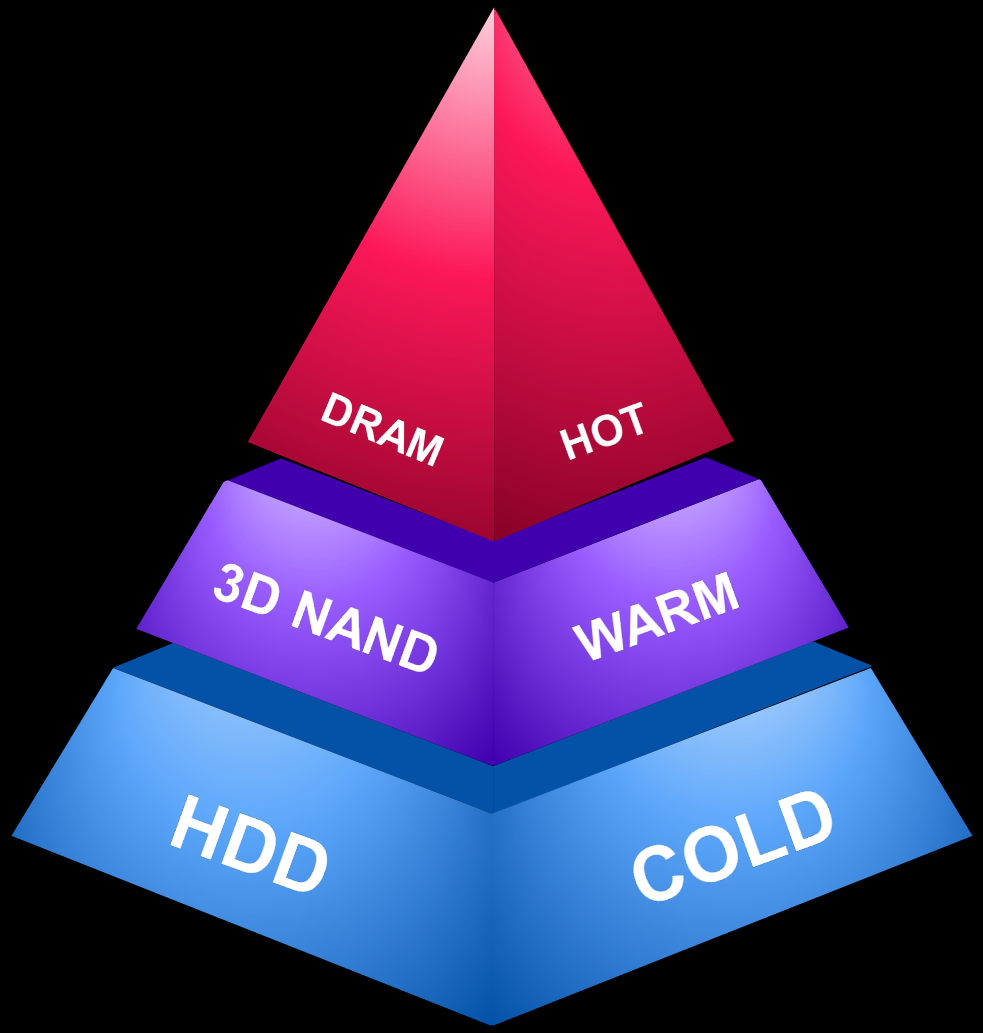
Memory an increasing % of system power and cost

- Memory price (cost/bit) flat due to scaling challenges
- Memory power scaling with speed

Price per Gb Log-Linear

Source : OCP Global Summit : “Software Defined Memory : A Meta Perspective”

2015s – Disrupting DRAM



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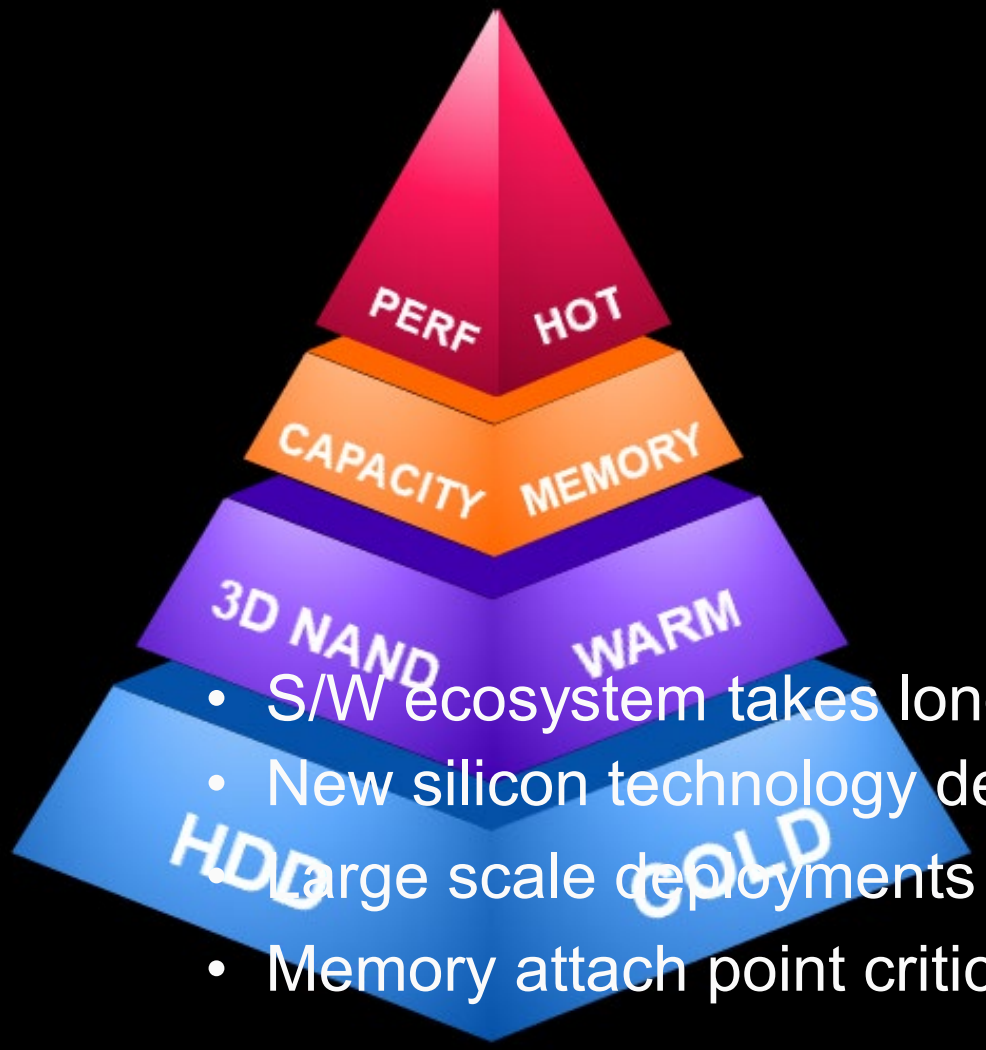
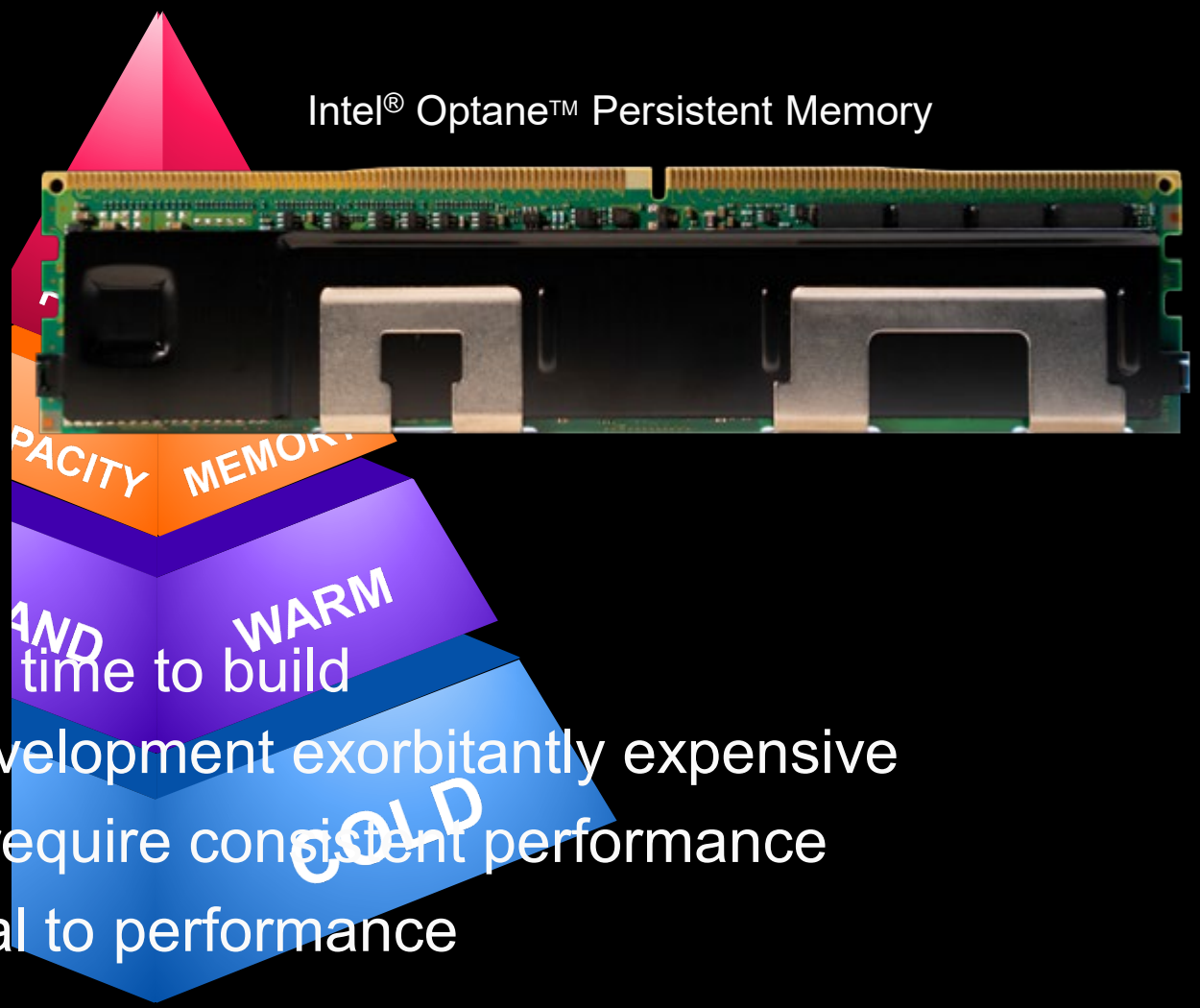
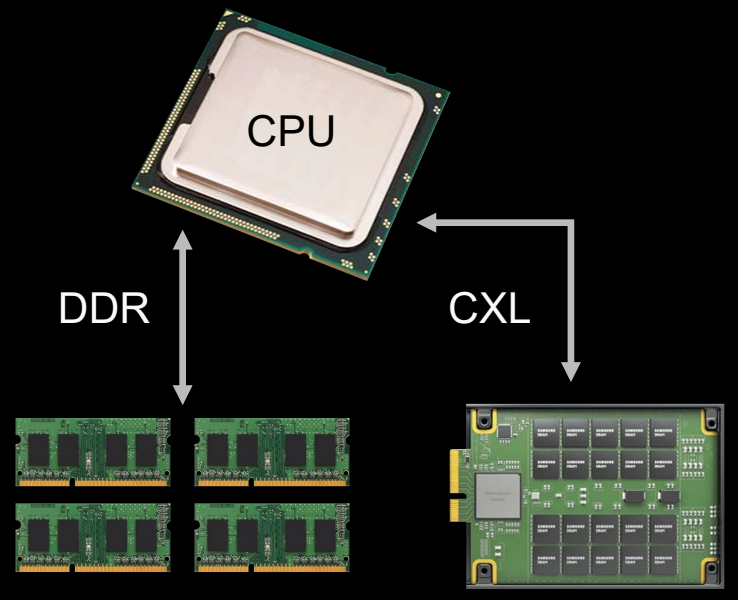




- S/W ecosystem takes long time to build
- New silicon technology development exorbitantly expensive
- Large scale deployments require consistent performance
- Memory attach point critical to performance

Solving Attach Point Problem : CXL

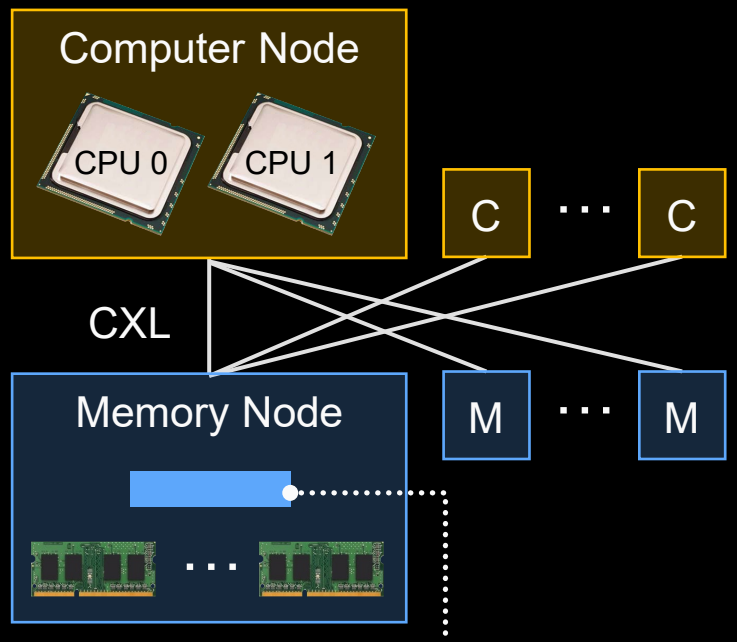
Direct Attached



Native DRAM

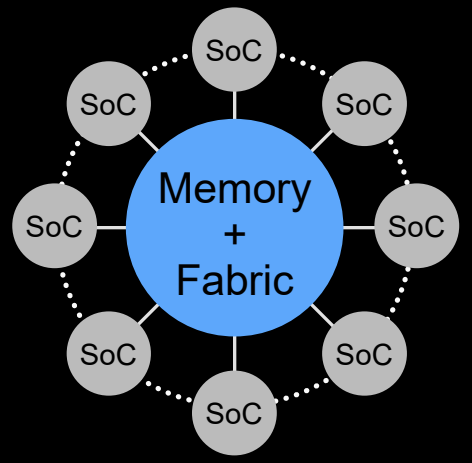
CXL Memory Module

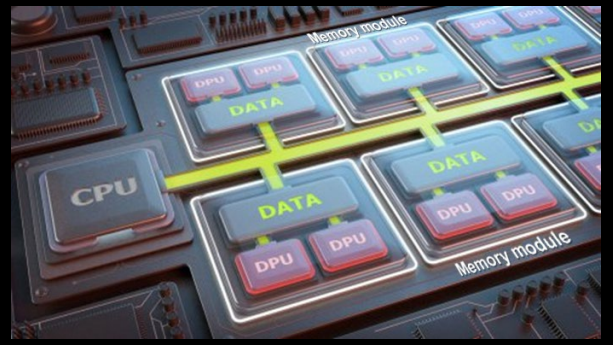
Memory Pooling and Sharing



CXL Pooling Memory Controller

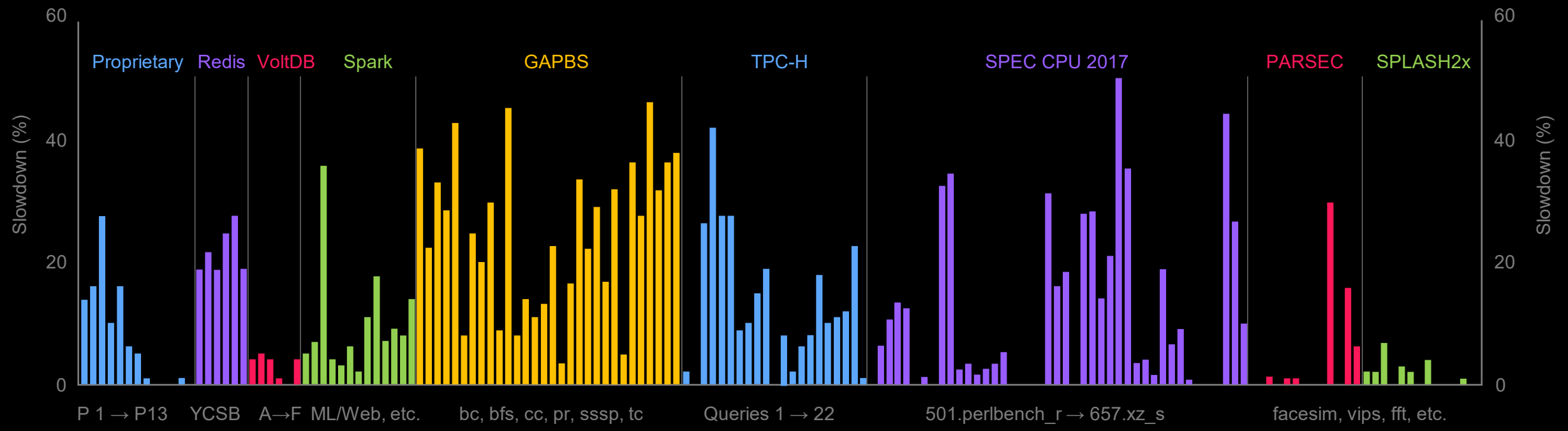
Memory Centric Compute





Performance with CXL-Attached Memory

Performance slowdown under additional 64ns memory latency

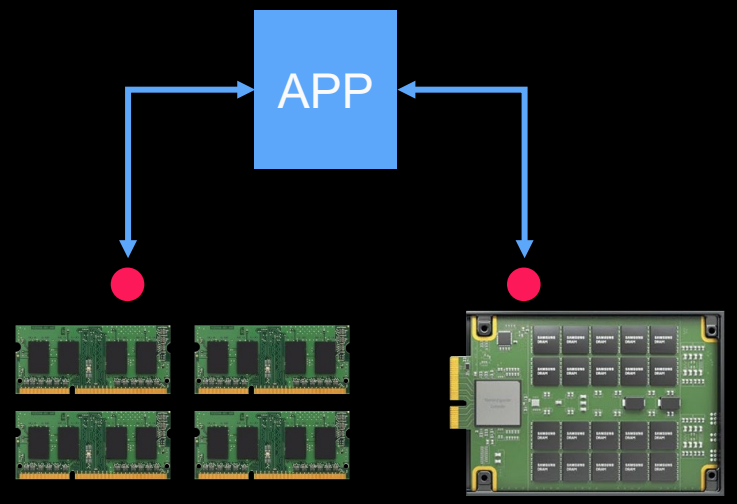


One size does NOT fit all

Source : First-generation Memory Disaggregation for Cloud Platforms, Huaicheng Li et al, Mar 2022

Solving The Performance Problem

S/W Driven



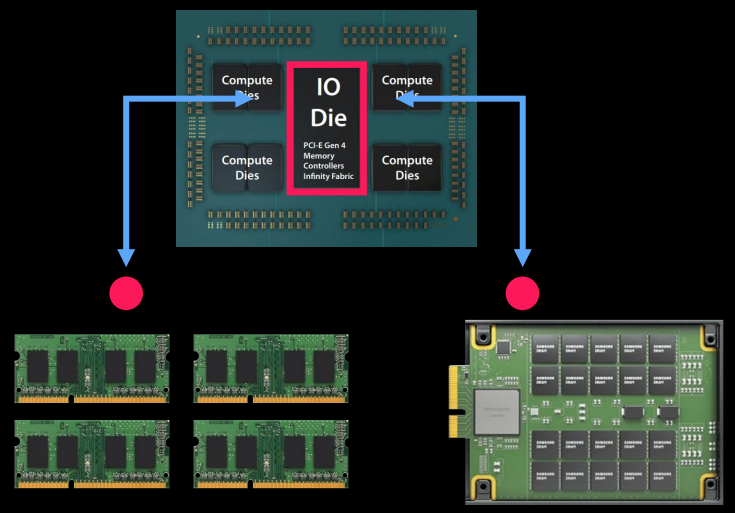
Native DRAM

CXL Memory Module

SAP HANA

pmem.io

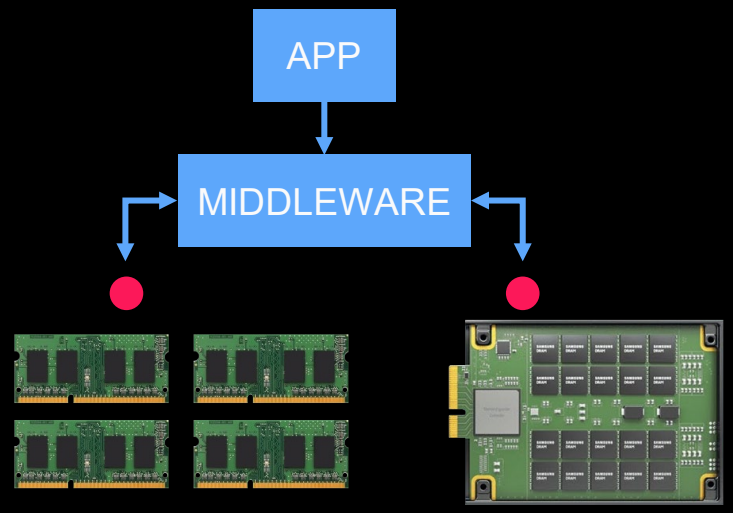
H/W Driven



Native DRAM

CXL Memory Module

M/W Driven



Native DRAM

CXL Memory Module

vmware

Google

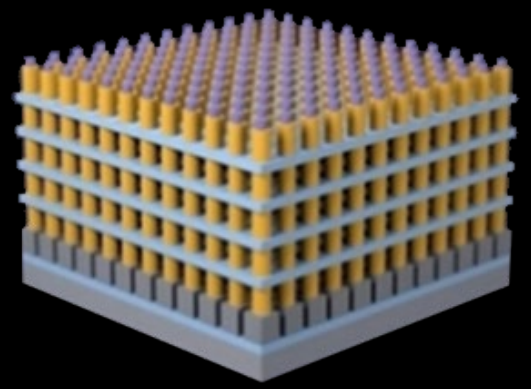
Meta

MemVerge

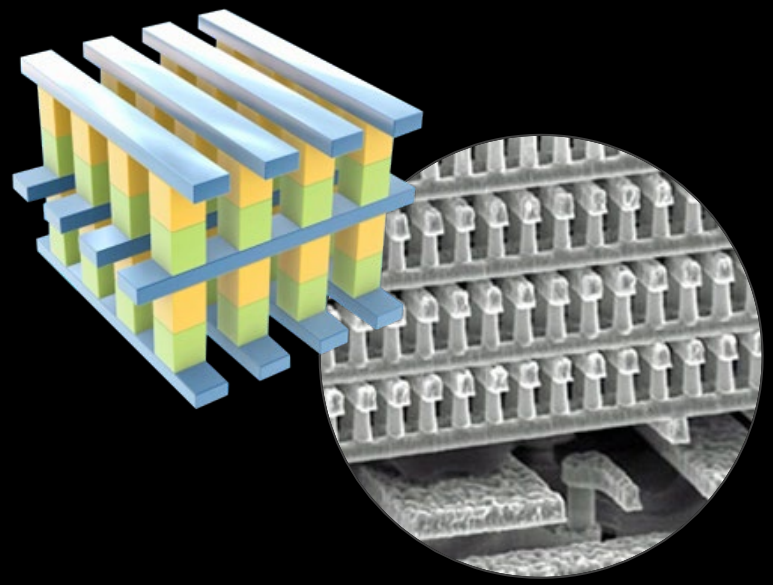
Microsoft Azure

Solving The Cost Problem

Conventional DRAM



Modified DRAM



New Memory Technology

Solving The Economics Problem

Incumbents

Venture Capital

Customers

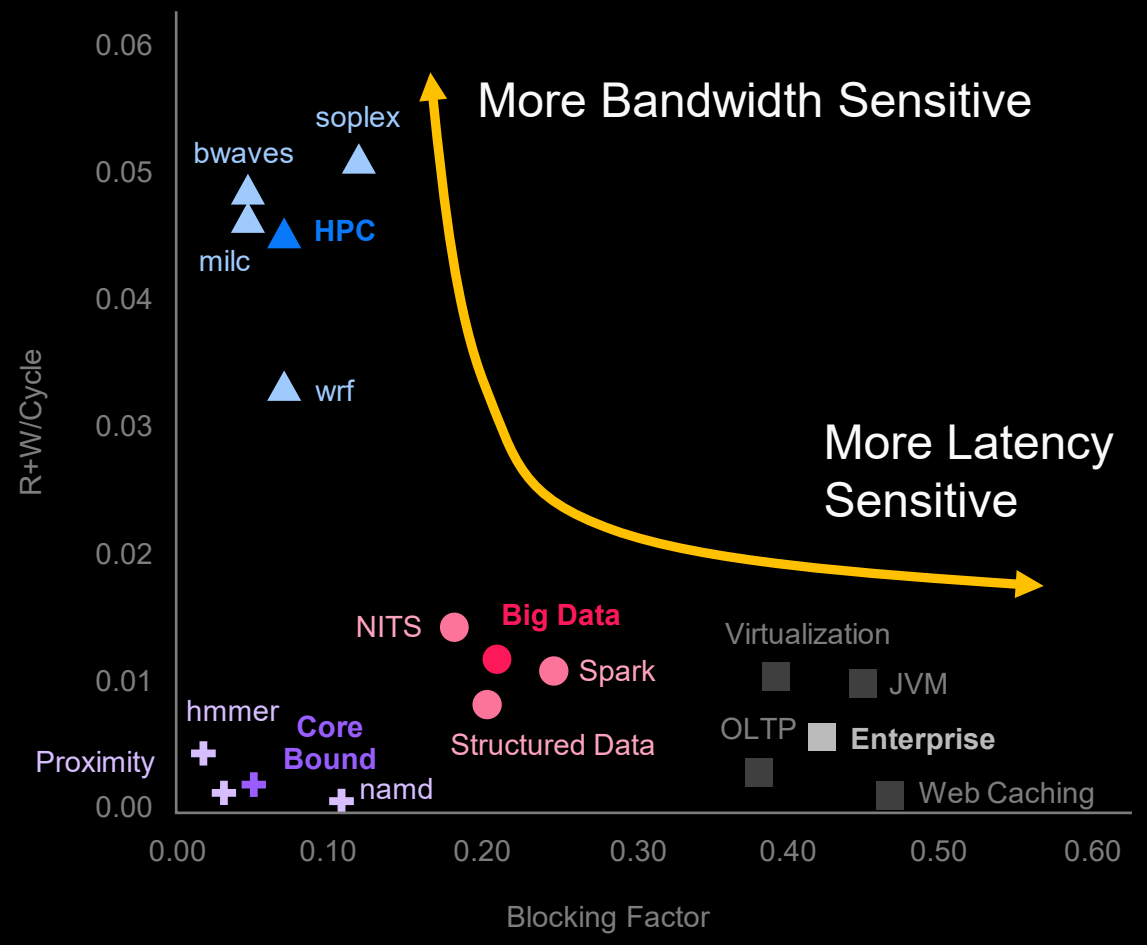
Government

Where will the tide take us?

Western Digital®

Create What's Next

Performance with CXL-Attached Memory



Bandwidth demand vs latency sensitivity

Source : Quantifying the Performance Impact of Memory Latency and Bandwidth for Big Data Workloads, Russell.M.Clapp et al, 2015 IEEE International Symposium