Test Challenges in Advanced Designs and Technology

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cadence®

Overview

- Today’s designs require knowledge and co-optimization of test and design
- Test offers new differentiators to the design flow for high reliability and safety-critical applications
- An integrated test and design flow delivers the least power, area, congestion, and timing impact while minimizing test time

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Advanced Design and Test

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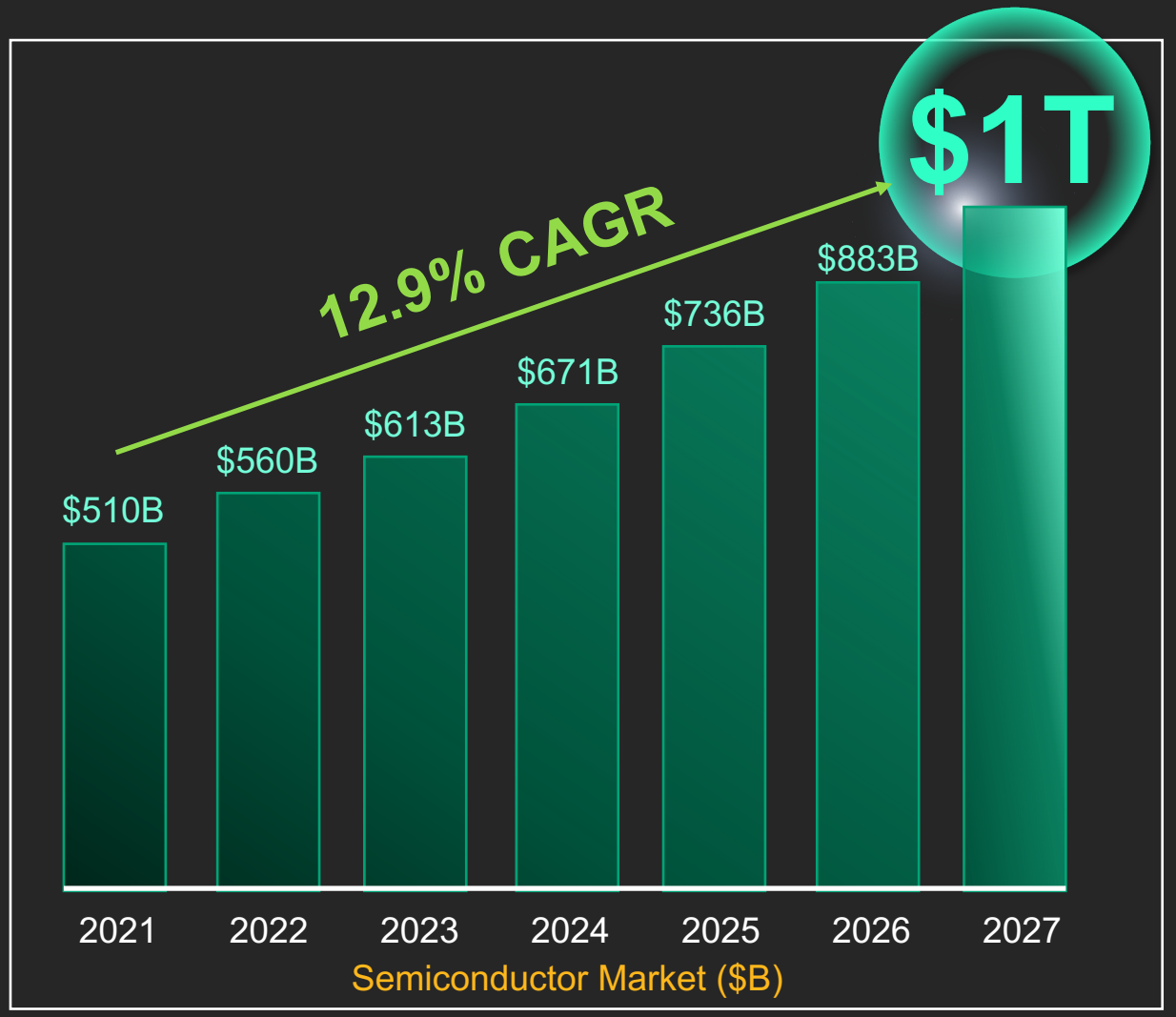
Exciting Growth for Semiconductor



Source: Impact of AI on Semiconductors, International Business Strategies (IBS), February 2022

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What's Driving Semiconductor Growth?

Automotive

50% EVs
U.S. Gov't 2030 initiative

$1200 BOM
semiconductors per car

19TB/hour
generated vehicle data

Source: Omdia AMFT Q1 2022

Hyperscalers

1,500ZB
blobal data generated in 2027

50X
ML model complexity growth every 18 months

$45B
2027 AI processors revenue

Source: Synergy Research Group (SRG) Dec 2020 and Cadence estimates

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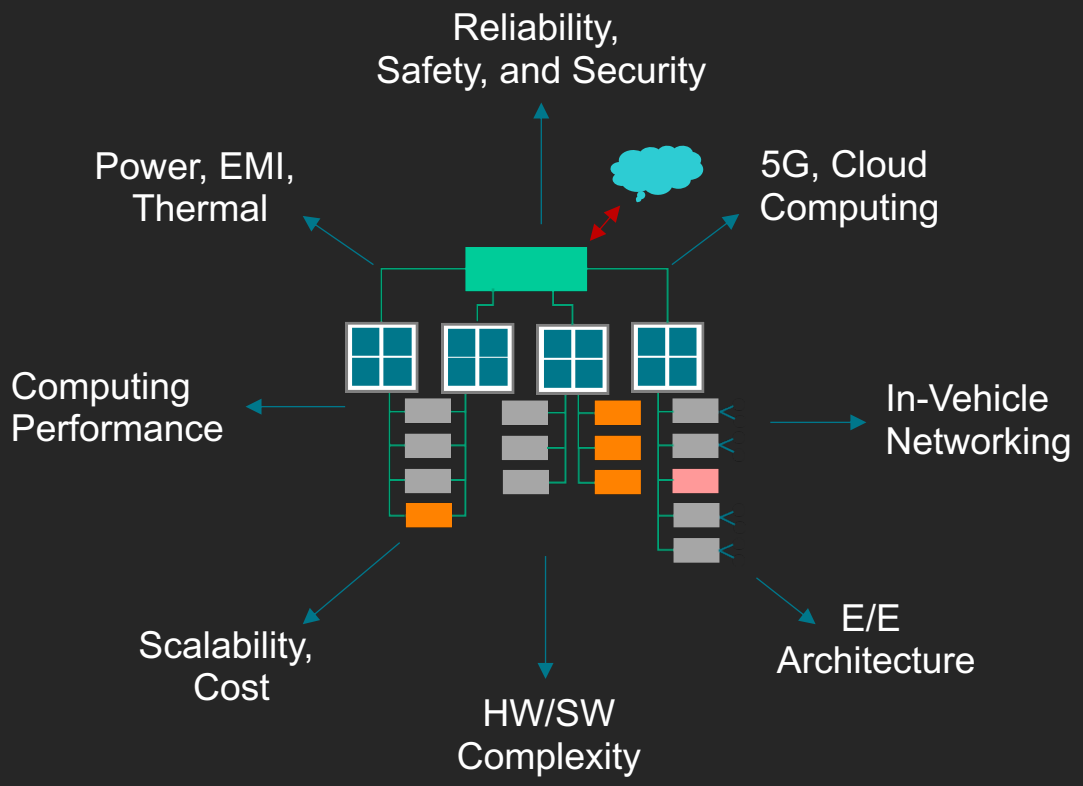
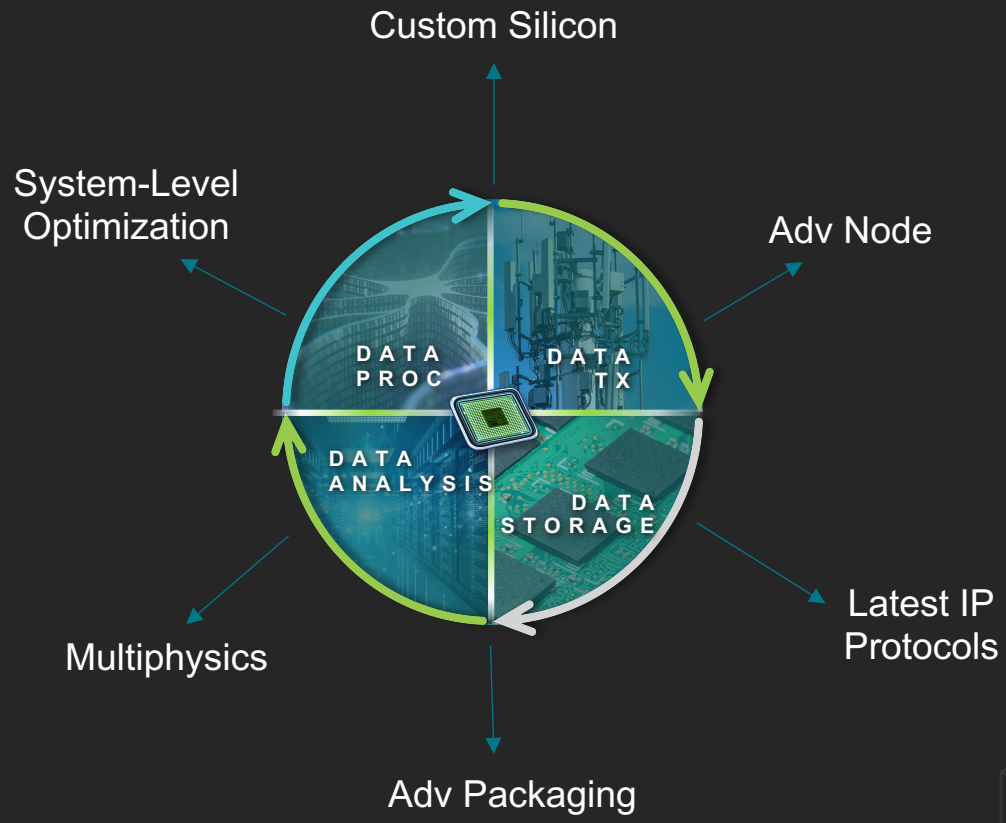
Enabling Technology Is Critical to Sustain Growth

Automotive



Hyperscalers



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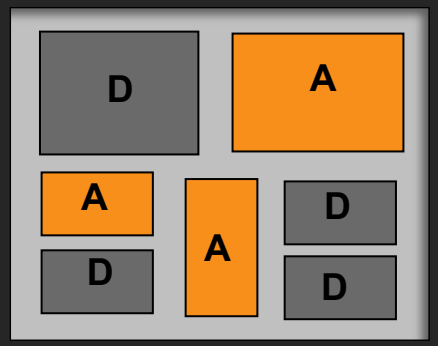
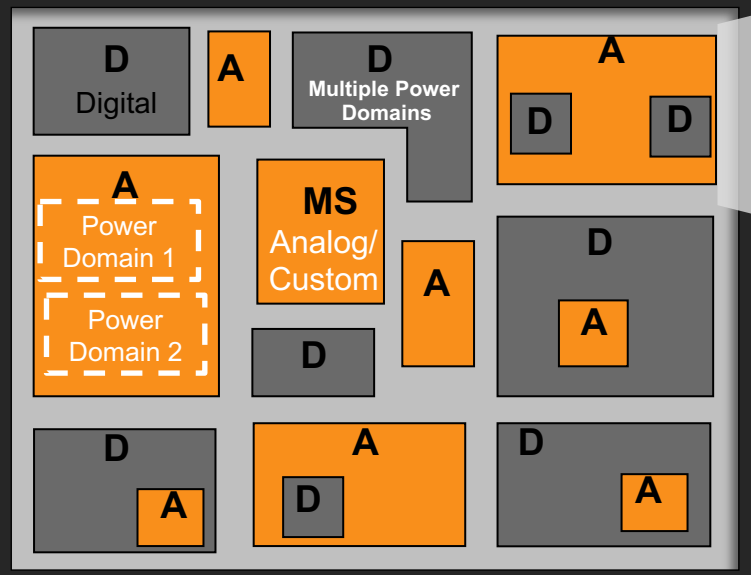
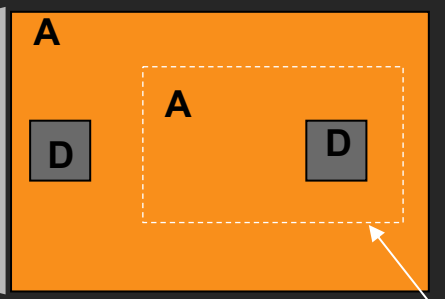
Mixed-Signal Design Trends – Flexibility and Interoperability

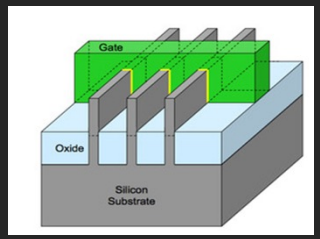
Traditional MS designs



Today's MS designs







Physical Hierarchy

Test challenge:
How to integrate and program mixed-signal IP?

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Test Challenges

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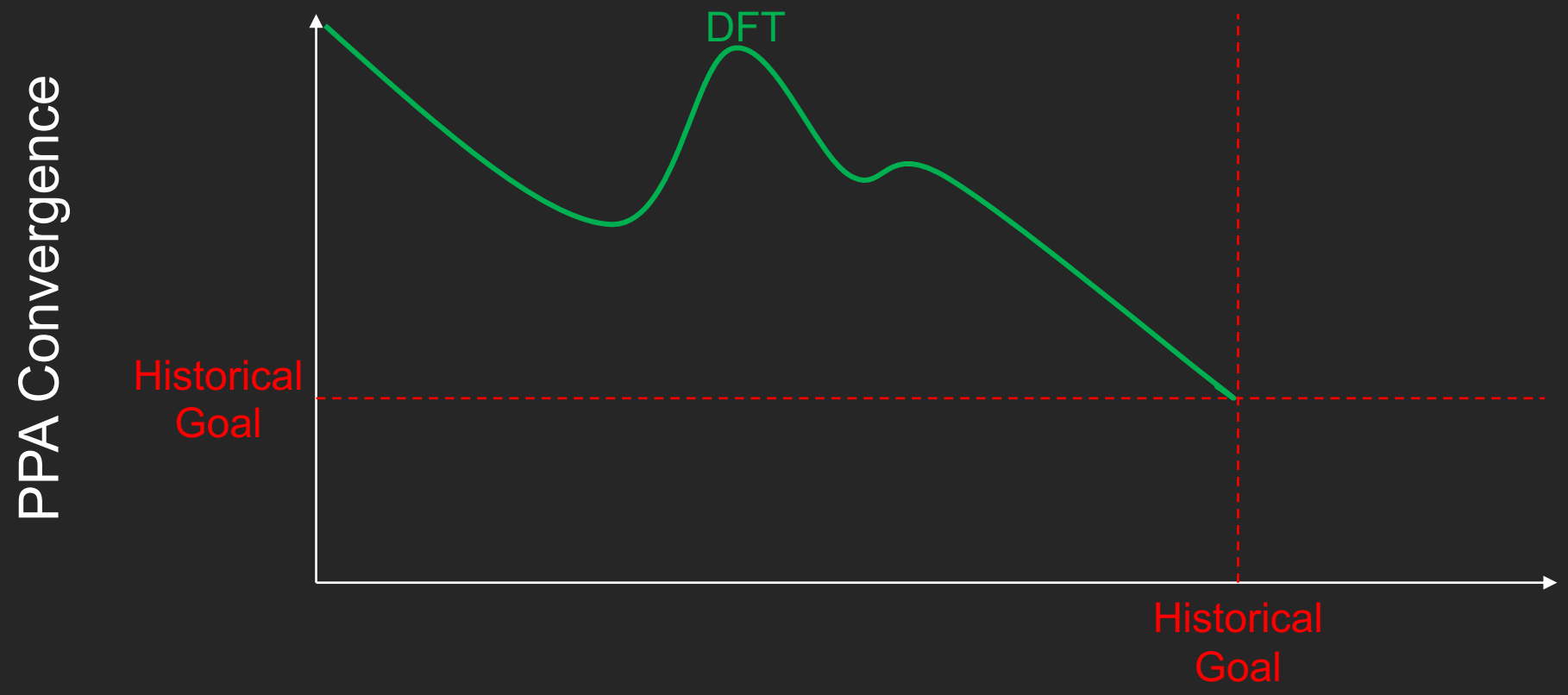
Design Convergence and Test – Historical View



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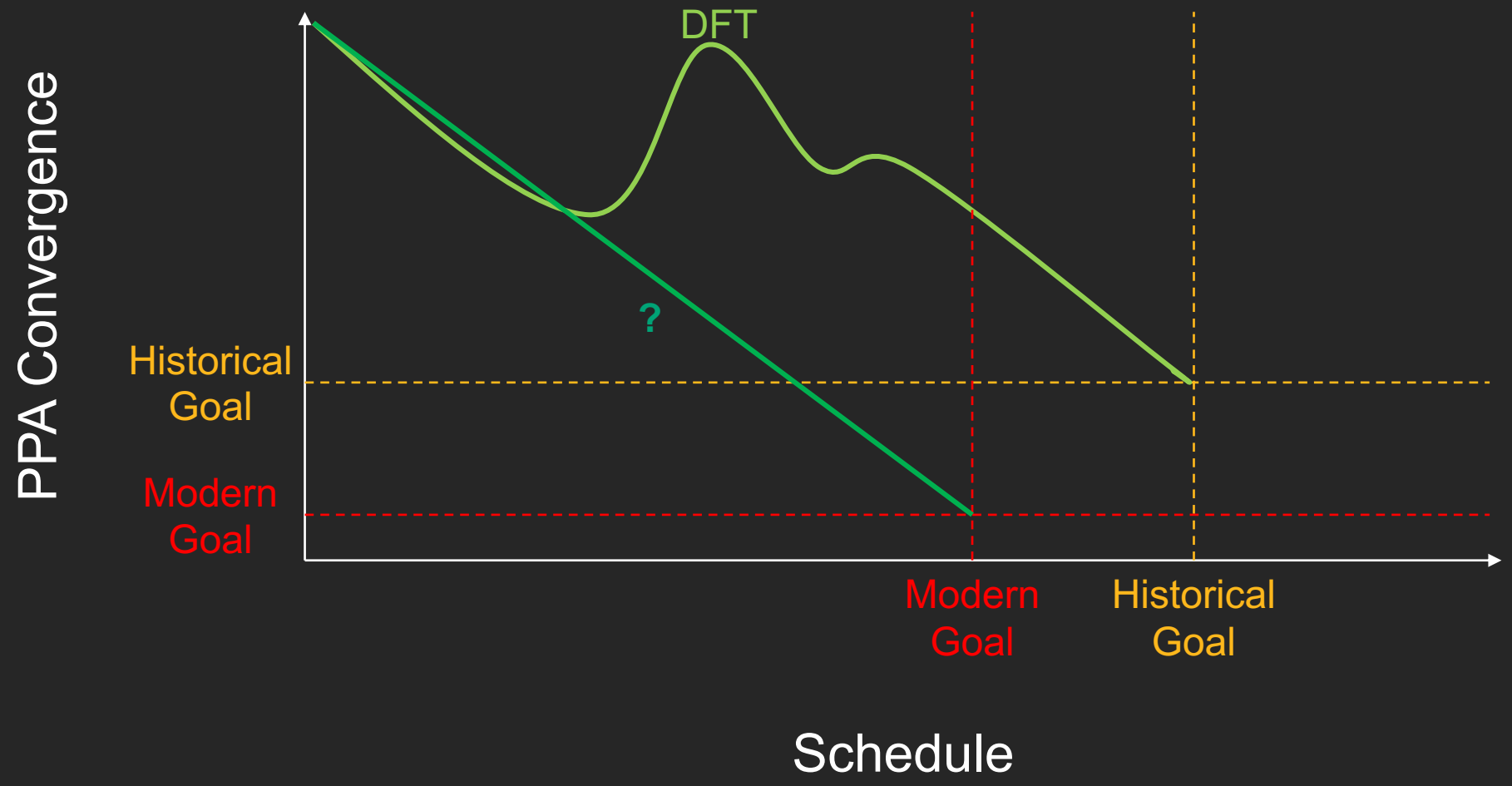
Design Convergence and Test – Modern View



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Test Challenges

- Test and physical design
- Analog design test requirement
- Test points without PPA impact
- Test-aware ECO

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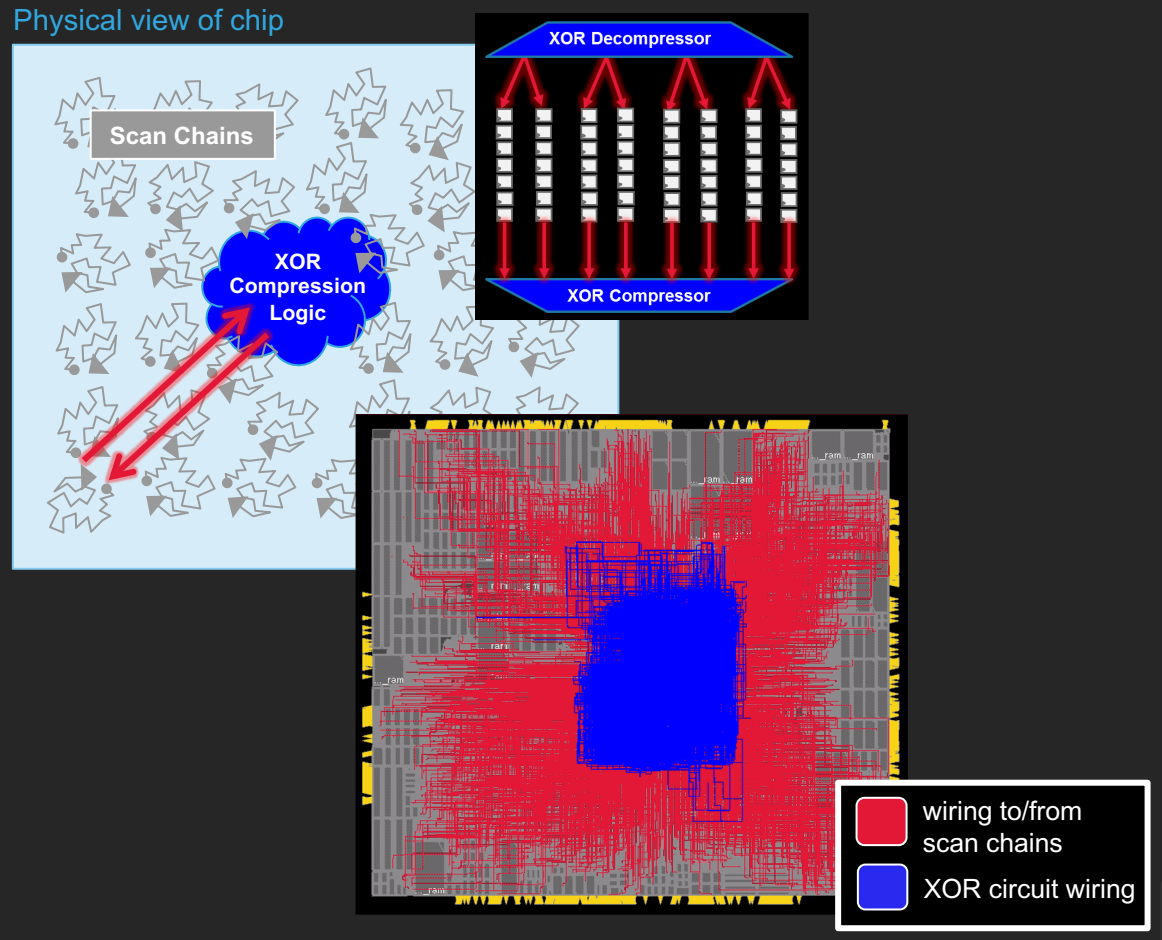
Test and Physical Design Impacts – Existing Solutions

- Routing congestion
  - Example: Scan compression logic
- Power, timing, and area impacts
  - Example: BIST logic



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Test and Physical Design – New Solutions

- Innovus™ and Virtuoso® solutions – Gold standard for physical design

- Test integrated with design flow – optimize inside the flow, not outside
  - Example: Modus 2D Elastic Compression

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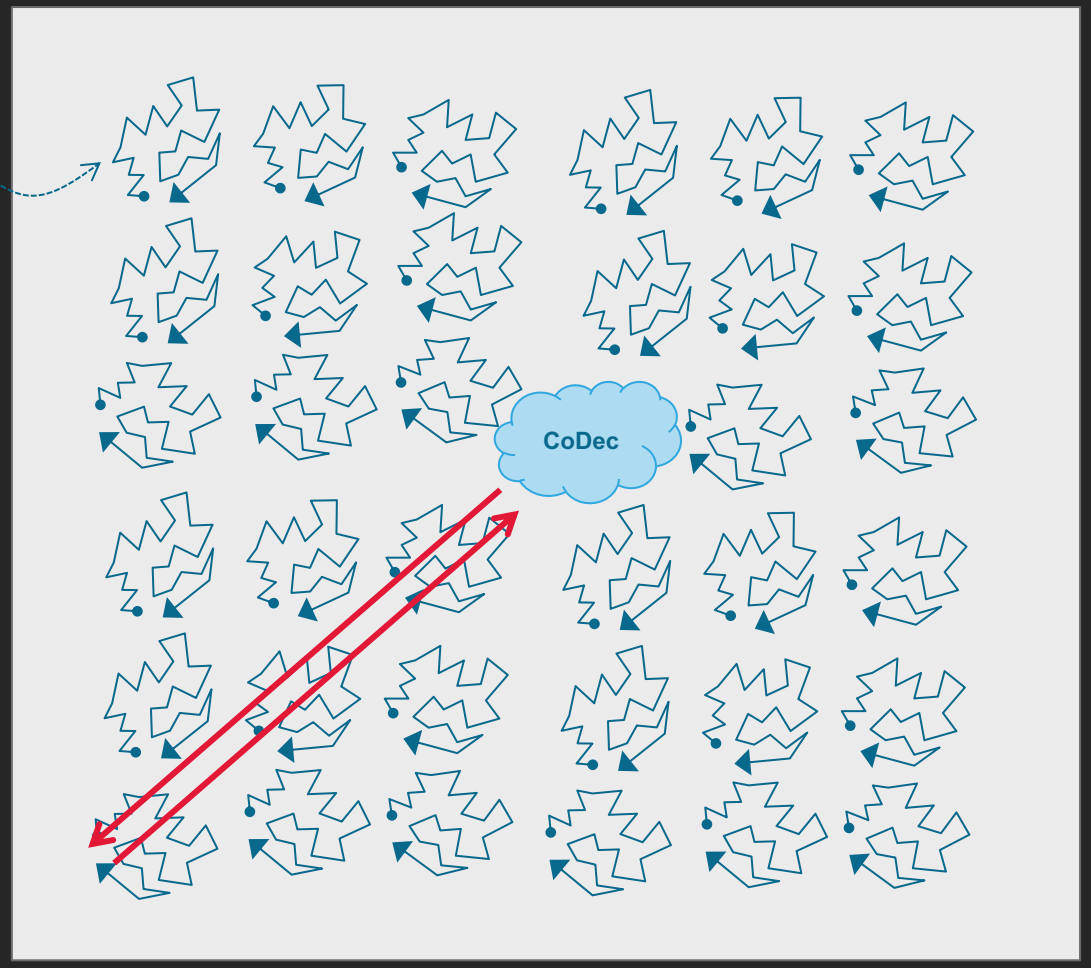
Routability as a Compression Limiter – Traditional Routing

Physical view of chip



More channels = more wirelength to/from CoDec

- CoDec logic (compression and decompressor) placed in middle of the design
- Scan channel heads/tail wires are fed from/to CoDec
- As more channels are added the more channel head and tail wires are needed
- Creates “cross-bar” congestion

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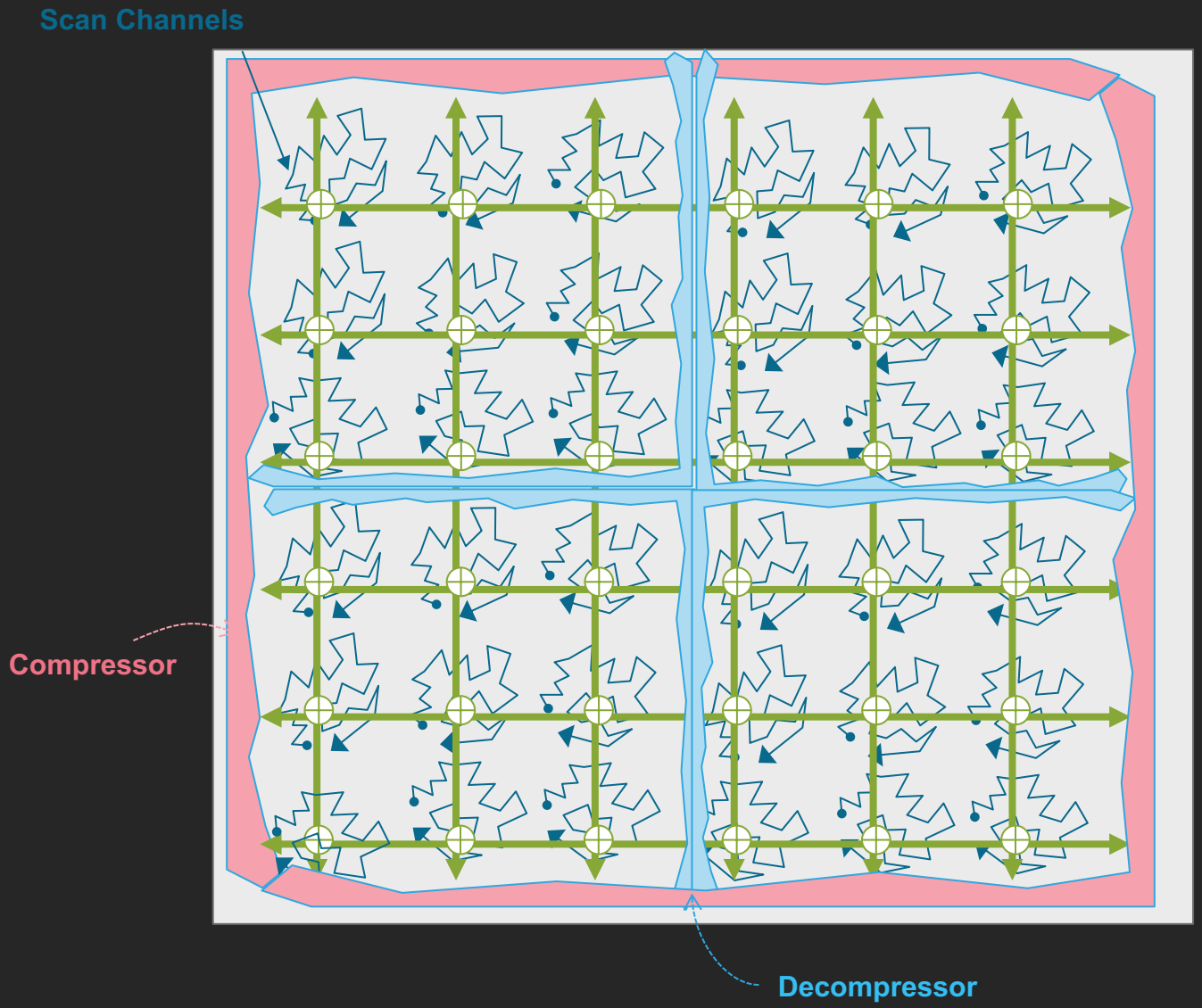
Cadence 2D Compression



- CoDec spread throughout the design
  - Grid structure spread compression scan data
- Connects locally with the scan channel heads/tails to minimize wiring
- Grows with the compression ratio to ensure local scan channel connections
- Less growth than using a centrally located CoDec and removes “crossbar” congestion

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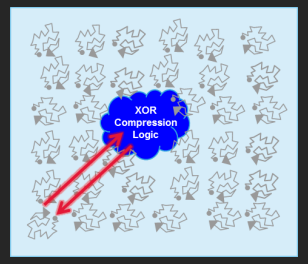
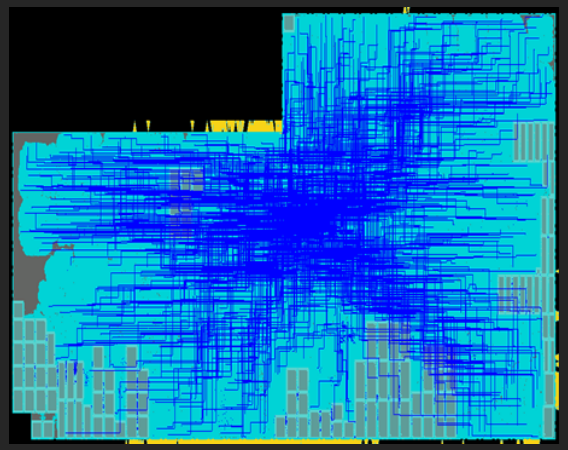
Industrial Results – 2D Compression

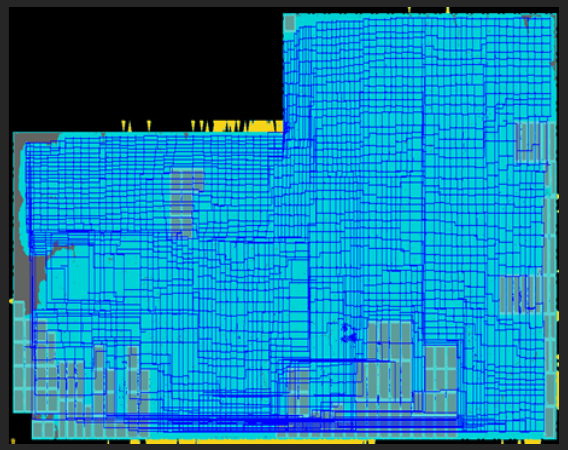
- 2D compression logic forms a 2D grid across the chip
- Up to 2.6X less routing resource than traditional 1D XOR compression

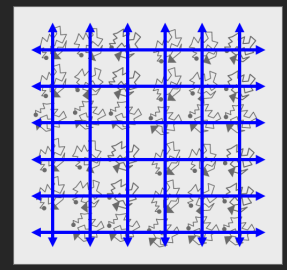
Traditional “1D” XOR Compression at **100X**





Modus 2D Compression at **400X**





Industrial example:
14.35% lower scan wirelength, 1.38% lower total wirelength, 1.26% lower density,
Consistent TNS improvement

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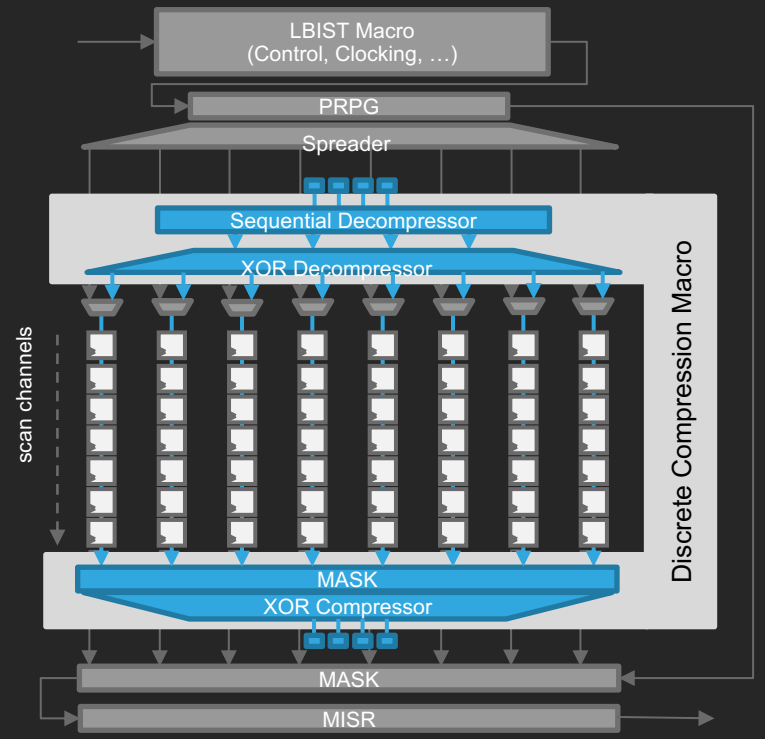
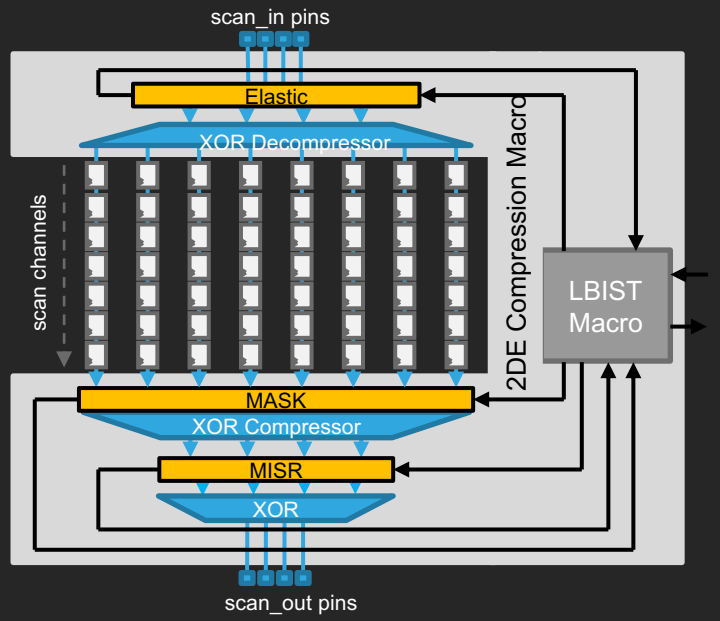
Logic BIST and Scan Compression – Extending 2D

- Traditional – Discrete
  - Cell area and routing penalty
  - Cannot achieve short channels due to routing congestions



- Unified LBIST and 2D Scan Compression
  - Brings physical benefits of 2D grid to LBIST
  - Shorter channels = faster LBIST
  - **47%** lower area, **75%** less routing, **50%** faster LBIST



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Example: IoT Medical

- Requirements:
  - **Heavy mixed-signal content** – cannot separate digital/analog cleanly
  - **Ultra-low power** – longer battery life
  - **Advanced process nodes** – new reliability and quality challenges
  - **Complex packaging** – silicon/package/board co-design

- Test challenges:
  - Lower power from in-system test
  - New fault models and test cost mitigation
  - Mixed-signal and packaging test constructs and methodology
  - Integration with custom and standard cell-based physical design

AMS circuitry typically occupies 20% of the area but incurs
70% of the test cost and 45% of the DFT/test effort

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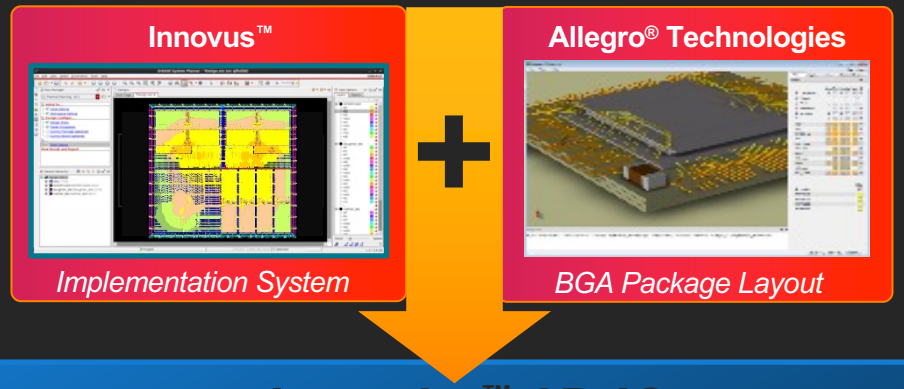
Integrity 3D-IC – Integrating Leading P&R and Package Solutions



- Integrated 2.5/3D design planning and implementation
  - Multi-Die
  - Interposer
  - Package
- Multi-die capacity
- Enables co-design with Innovus, Virtuoso®, and Allegro platforms
- 3D analysis and signoff to enable system-driven PPA
- Full integration with **Modus DFT/ATPG**

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Mixed Signal Test – Standardization and Automation

Moving into the future

- Standard for describing **analog test access and control** (IEEE P1687.2)
  - Address issue with IP integration and mixed signal complexity
  - Build off IEEE 1687 ICL/PDL

- Standard for analog **defect modelling and coverage** (IEEE P2427)
  - No universally accepted fault models as in digital
  - Analog test becomes defect-oriented structural approach, based on defect models

Automation Only Possible with Standardization

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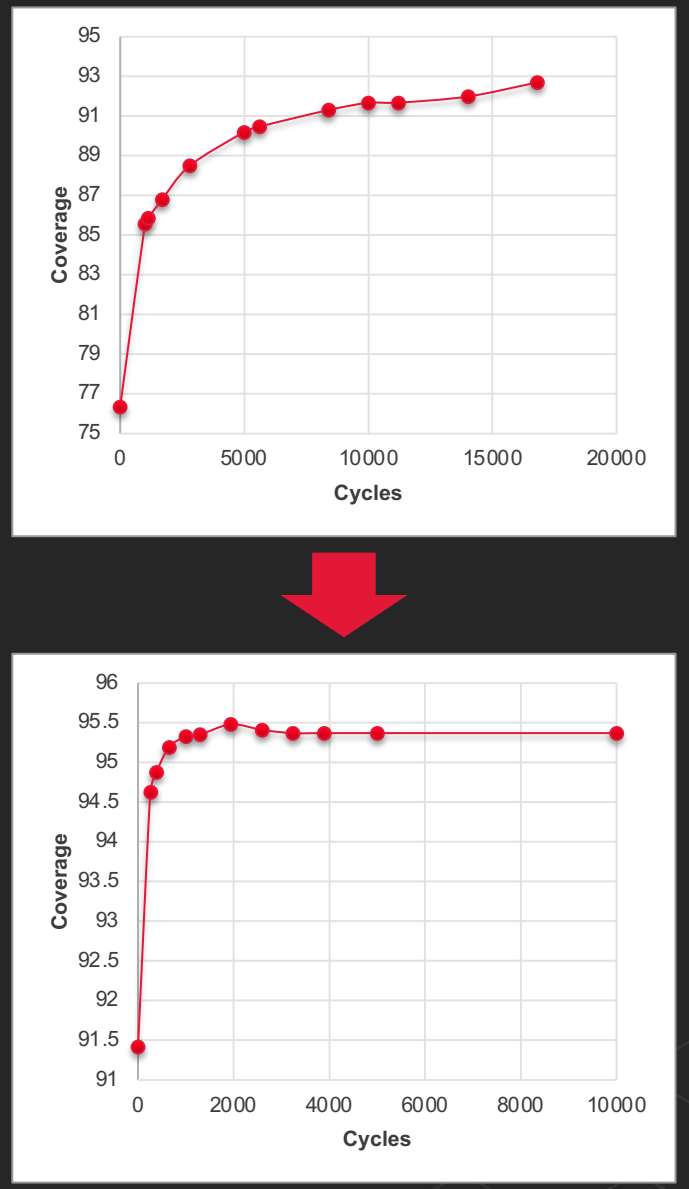
Test Points

- Surgical modification of logic to meet a test goal
  - Observe/control
- Examples:
  - Improved LBIST coverage
  - Meet delay test goals without test cost explosion
- Requires design context – **power, area, timing**
  - Common engines with physical design
  - Risk disturbing existing design convergence



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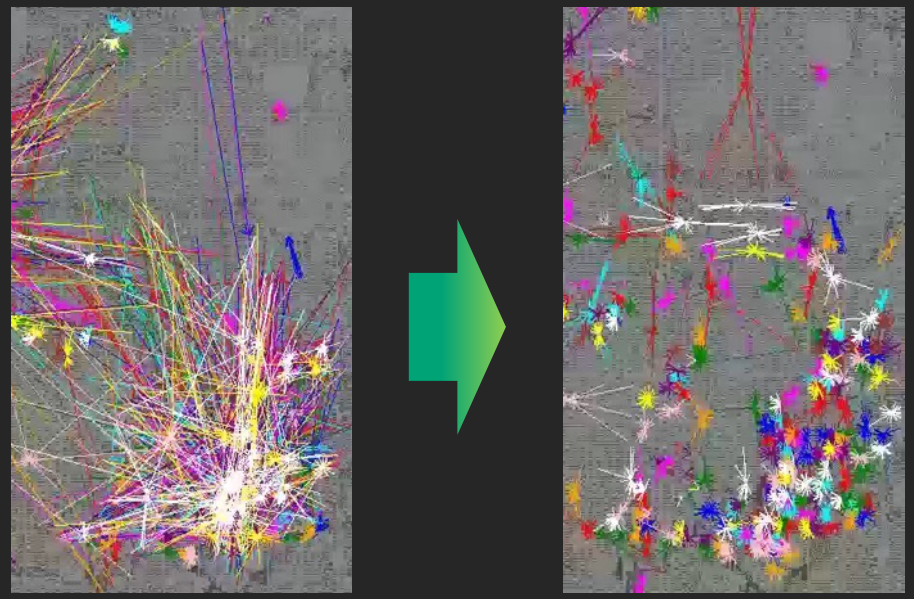
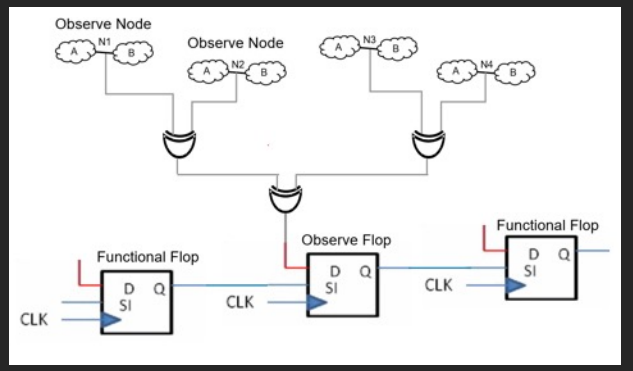
Physically Aware Test Points – Modus and Innovus

Area and routing congestion solution for test-critical designs

- Sharing control and observe test points – reduces # TPI needed
- Repartitioning the test points when the design is optimized in iSpatial and Innovus™



Industrial example:
4X improvement in TPI wirelength



Genus™
- syn_gen -phys
- syn_map -phys
- Identify Test points
- Insert Test points
- Scan insertion
- iSpatial
  - GigaPlace GigaOpt

Modus
- ATPG

Shared Control and Observe Test Points

Physically Aware Test Point Optimization

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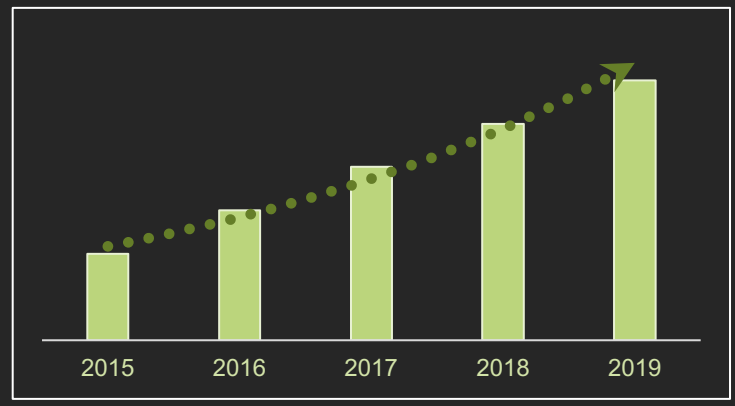
Test-Aware ECO

- ECO is part of the mainstream design process
  - Enables faster design closer
  - Addresses design issues with limited PPA impact
- Test logic required to be preserved and validated through ECO process
  - Required for minimal design change
  - Traditionally a manual process to re-stitch test logic

Growing trend of Functional ECOs



- **Conformal® ECO – Industry-standard ECO**
  - Automatically preserves original scan chains
  - Validates scan chain correctness
  - Extensible to other test logic

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Test in Full Flow

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Best-in-Class Analog and Digital Design

- Cadence has dominance in both analog and digital implementation
  - Innovus™ Implementation – Physical design platform of choice for advanced node designs
  - Virtuoso® Platform – Industry gold standard for custom design
  - Conformal® ECO –Tthe only solution for automating complex ECOs
- Native bridge between analog/digital – MSOA
  - Seamless editing in cockpit of choice
  - Tempus™ Timing – Mixed-signal STA
  - Voltus™/Voltus-Fi Power – Full SoC power integrity

The Flow of Choice for Test Integration

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Summary

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