Open-Source Has a Great Price
But Verification Adds the Real Value

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Agenda

• Introduction
• RISC processors are not new, so what is new about RISC-V?
• RISC-V processor design verification (DV) challenges
• Stepping up to the challenge, it takes an ecosystem...
• Latest progress on the new RISC-V Verification Ecosystem and new standards
• Summary
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Imperas Founding Story

• Imperas founding team has background in Electronic Design Automation (EDA) tools, and FPGA and processor IP companies

• Imperas’ Founding Vision:
  • Embedded software development is ready to embrace simulation
  • As in EDA, specialized tools and methodologies are required
  • Tools should be developed starting from these domain-specific requirements

• Today:
  • RISC-V: software simulation and design verification
Imperas and RISC-V

- Q2 2016: Design Automation Conference – Imperas first learns about RISC-V – looks academic and fragmented
- Q4 2016: RISC-V Workshop (@ Google) – 350 attendees from serious companies, and the ISA looks to be converging
- Q1 2017: Imperas joins the RISC-V Foundation; builds first RISC-V processor model
- Q3 2017: Imperas starts participating in the Compliance Working Group; builds/donates ISS and tests
- Q1 2018: Imperas introduces methodology for adding/optimizing custom instructions (architecture exploration) for RISC-V cores
- Q2 2018: First paying customer using Imperas RISC-V models and tools for software development and design verification (DV)
- Q4 2018: First paying customer using Imperas RISC-V models and tools for architecture exploration
- Q1 2019: First tape out of RISC-V SoC based on using Imperas model as DV reference model
- Q2 2019: Imperas starts collaborating with Google on DV flows with instruction stream generator
- Q1 2020: Imperas starts working with the OpenHW Group and individual members on DV of Core-V cores
- Q1 2021: Imperas presents 2 papers on RISC-V processor DV at the DVCon Silicon Valley conference (with OpenHW, Nvidia Networking)
- Q4 2021: Imperas introduces ImperasDV RISC-V verification product line
- Q1 2022: Imperas introduced RVVI (RISC-V Verification Interface) as an open standard on GitHub for the RISC-V DV community
- Q3 2022: Imperas releases the first open-source SystemVerilog testbenches for the RISC-V Verification Ecosystem

We’ve been there since the start!
Imperas RISC-V Customers and Partners

The most complex RISC-V processor projects use Imperas

Users
- Nagravision
- Nvidia Networking (Mellanox)
- EM Micro US
- Silicon Labs
- Dolphin Design
- Seagate Technologies
- lowRISC (Ibex)
- RISC-V processor IP vendor
- Top-tier systems company (AI application)
- Top-tier consumer electronics company (AR/VR application)
- NSITEXE (DENSO subsidiary)
- Startup building accelerator based on multiprocessor RV64
- Japanese government projects “TRASIO” and “RVSPF”
- Barcelona Supercomputing Center
- Numerous universities around the world

Partners
- RISC-V Intl (compliance, bitmanip, crypto, various events)
- OpenHW (verification working group)
- CHIPS Alliance (verification working group)
- Google (for open source ISG, & co-author DV papers)
- Valtrix (test generation tools)
- Andes (processor IP vendor)
- SiFive (processor IP vendor)
- Codasip (processor IP vendor)
- MIPS (processor IP vendor)
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RISC-V History

• An open standard ISA (Instruction Set Architecture) that began in 2010 at the University of California, Berkeley
• Provided under a permissive license, now managed by RISC-V International
• Modular Instruction set framework designed for flexibility and adaptability
• RISC-V specification allows developers to
  • Select pre-defined extensions (eg multiplier, vector) with configuration options
  • Plus add custom features with optimized instructions and extensions
  • Design freedom for processor configuration and optimization
    • While maintain combability with the supporting ecosystem of OS/RTOS, Tools and Software
• Its this freedom, and not the free, as to why RISC-V usage is growing so fast
Freedom Enables Domain Specific Processing

• RISC-V is growing in market segments where x86 (PCs, data centers) and Arm (mobile) architectures are not dominant
  • Small microcontrollers for SoC management, replacing proprietary cores
  • Verticals such as IoT and AI/ML
  • Horizontal markets such as security

• RISC-V offers freedom to develop *optimized* domain specific processors

• RISC-V adopters include:
  • traditional semiconductor companies
  • embedded systems companies now developing own SoCs
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Challenges in RISC-V proprietary ISA IP vendors adoption

- Proprietary ISA single source processor IP companies
  - Arm, MIPS, Cadence (Tensilica), Synopsys (ARC), ...
  - Traditional proprietary ISAs have limited design options (freedom)
  - Fully pre-verified processor IPs ensures an ecosystem of support

- Their processor DV methodology is proprietary & brand value
  - including tools, reference model, test vector/suites

- Have the resources and expertise in processor verification

- Potential issues that could slow the adoption of RISC-V ISA
  - need to retool, build reference model and tests
Challenges in RISC-V Processor DV

- Feature selection and design choices require serious consideration
  - Must consider verification impact
- Current SoC cost is 50%-8x% for HW DV when using proven fully pre-verified CPU IPs (that’s all the effort _outside_ of the processor IP)
  - Developing new CPU adds incremental schedule, resource, quality challenges...
- Processor DV is a new challenge for many SoC development teams
- Existing SoC DV methodologies don’t completely address the challenge
- As of 2021, no commercial products available to support mass-market DV of processors

RISC-V represents the biggest migration of DV responsibility in EDA history
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  3) Methodology
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Collaboration

• Unique blend of open-source, non-profit, and industry contributions
• riscv-dv: random instruction stream generator (Google/CHIPS Alliance)
• core-v-verif: verification environment for RISC-V processors based on UVM (OpenHW Group)
• RVVI: open standard interface and API for RISC-V processor verification (Imperas/OpenHW Group)
OpenHW Group

- Open-source RISC-V Cores
- Industrial strength verification
- Commercial tools and methods
- CV32E40P now in commercial use
- Future roadmap needs
  - High quality verification
  - Efficient reuse of VIP
  - Easy adoption across all teams
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Standardization

• Good for IP users and IP vendors
• For users:
  • Supports best practices
  • Reuse and portability
  • Get up and running faster
• For vendors:
  • Less configurability, better quality
  • Ease of customer support
• UVM standard is a good example
Standardization: RVVI

- RVVI = RISC-V Verification Interface
  - [https://github.com/riscv-verification/RVVI](https://github.com/riscv-verification/RVVI)
- Work has evolved over 2 years
  - Imperas, EM Micro, SiLabs, OpenHW
- Standardize communication between testbench and RISC-V VIP
- Two parts:
  - **RVVI-TRACE**: signal level interface to RISC-V VIP
  - **RVVI-API**: function level interface to RISC-V VIP
RVVI-TRACE

- Defines information to be extracted from the RISC-V core by tracer
- SystemVerilog interface
- Includes functions to handle asynchronous events
  - E.g. interrupts, debug req

- Standard functions that RISC-V processor VIPs need to implement
- Supports a step-and-compare methodology
- C and SystemVerilog versions available
- [https://github.com/riscv-verification/RVVI/blob/main/include/host/rvvi/rvvi-api.h](https://github.com/riscv-verification/RVVI/blob/main/include/host/rvvi/rvvi-api.h)
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Methodology

• Best practices designed to address a known problem
• Built on experience
  • Learnings from past successes and failures
  • Hit the ground running
• Imperas is working to establish RISC-V processor DV methodology
  • Collaboration with customers and ecosystem partners
• Result: Asynchronous step-and-compare
Asynchronous Step and Compare

• Stimulus:
  • Directed and constrained-random tests
  • Random Instruction stream generator

• RISC-V Reference model:
  • High-quality, validated, instruction-accurate processor model
  • Configurable to match processor customizations
  • Runs same software as DUT
  • Able to respond to asynchronous events
Async Step and Compare (2)

• Comparison:
  • DUT and reference model run in lock-step
  • Internal state completely compared at each significant event
    • E.g. instruction retirement, trap
  • Errors reported immediately
  • Supports multi-hart processors and out-of-order and multi-issue pipelines

• Functional coverage:
  • Instructions, registers
  • Sequences and scenarios of interest
  • Asynchronous events
OpenHW CV32E40P

Success!

But that was a lot of work... and now needs to scale across the roadmap of cores
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Verification IP

- Get a head start
- Benefit from knowledge, experience of others
  - Adhere to standards (eg RVVI – RISC-V Verification Interface) and support best practices
- Save time and resources
- High quality
- Customer support

- You don’t have to be a RISC-V expert to verify a custom RISC-V processor
ImperasDV: RISC-V VIP

- Supports RVVI natively
- Supports async step-and-compare
- Supports random instruction streams
- Supports async events
- Manages synchronization and performs all comparison and checking
- User implements the tracer block
  - Using RVVI guidelines

https://www.imperas.com/ImperasDV
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Imperas is the Reference Model

- Imperas provides full RISC-V Specification envelope model
- Industrial quality model /simulator of RISC-V processors for use in compliance, verification and test development
- Complete, fully functional, configurable model / simulator
  - All 32bit and 64bit features of ratified User and Privilege RISC-V specs
  - Vector extension, versions 0.7.1, 0.8, 0.9, 1.0
  - Bit Manipulation extension, versions 0.91, 0.92, 0.93, 1.0.0
  - Hypervisor version 0.6.1
  - K-Crypto Scalar version 0.7.1, 1.0.0
  - Debug versions 0.13.2, 0.14, 1.0.0
- Model source included under Apache 2.0 open source license
- Used as reference by:
  - Mellanox/Nvidia, Seagate, NSITEXE/Denso, Google Cloud, Chips Alliance, lowRISC, OpenHW Group, Andes, Valtrix, SiFive, Codasip, MIPS, Nagra/Kudelski, Silicon Labs, RISC-V Compliance Working Group, ...

http://www.imperas.com/riscv
riscvOVPsimPlus
www.OVPworld.org/riscvOVPsimPlus

Imperas is used as RISC-V Golden Reference Model
Imperas Model Extensibility

Imperas develops and maintains base model
- Base model implements RISC-V specification in full
- Fully user configurable to select which ISA extensions
- Fully user configurable to select which version of each ISA extension
  - Updated very regularly as ISA extension specification versions change
- Fully user configurable for all RISC-V specification options
  - e.g. implemented optional CSRs, read only or read/write bits etc...

Imperas provides methodology to easily extend base model
- Templates to add new instructions
- Code fragment for adding functionality
- 100+ page user guide/reference manual with many examples
  - Includes example extended processor model

**Imperas RISC-V model is architected for easy extension & maintenance**
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- RISC-V processor developers need to do comprehensive verification of the RTL implementation, which represents a massive shift in verification responsibility.
- Open standards like RVVI (RISC-V Verification Interface) are essential to enabling efficient methodologies and advancing the RISC-V ecosystem.
- Asynchronous step-and-compare is the most comprehensive, most efficient RISC-V DV methodology based on leveraging SoC DV flows and resources.

The RISC-V Verification Ecosystem is ready to support the growth in RISC-V adoption.
Thank you

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