AI semiconductor clearly sees a strong momentum

AI chip technology is evolving rapidly, Gartner estimates that more than 50 companies are making chips specifically for AI, and AI-specific chip revenue is expected to reach $76.8 billion by 2025.
Let’s look at several key trends for AI SoCs

- **Accelerator-based designs:** Domain Specific IP for training and inference work more efficiently than general-purpose CPUs and GPUs.

- **AI at the Edge:** Growing trend towards processing AI workloads at the edge prioritize low-power and smaller die size.

- **Memory Architecture:** Reduced Latency is the holy grail in AI workloads. Chip designs are increasingly focused on optimizing memory architecture/choices.

- **Hybrid architectures:** Migration of AI chips using combination of different types of accelerators to optimize performance for specific AI workloads – chiplet opportunity.

- **Increasing performance:** Demand for performance of AI chips (training), both in terms of die size, raw compute power and energy efficiency are driving innovation in chip design, materials science, and cooling technology.

Source: GSA AI whitepaper, Dell

Choosing the Correct Memory: Comparison Data

Source: Rambus
The AI Chip Revolution has begun.....

More effort and partnership collaboration is required to realize IDEAS and INNOVATION into Silicon
So...Can I OWN my AI?

Cost of designing custom silicon is too prohibitive

$$ - EDA tools, IP licenses, people.....

Too much risks – unproven IP, new design flows etc

I don't have the right team

I need to have my silicon in months and not years

It's just too hard!

Multi touch points (EDA, IP, Foundry, OSATs etc...)
We need to get more specialized chips… but we cannot!

Upfront IP License $5M
Design NRE $10M
Fab cost $5M

$20M+

No way I can risk $20M upfront and spend 2 years before I get the first MVP!
Is there opportunity to reduce duplicated efforts?

**On Chip Owner**
- Application Specs
- Custom Domain IP
- SoC Specs
- Architecture
- Key IP Configuration
- Verification Requirements
- HW/SW Bring-up

**On Design House**
- Physical Implementation
- Physical Design
- PKG

Colors:
- Green: Unique Value
- Orange: Duplicated Efforts
- Blue: Dependency
Need to Dramatically Enhance Design Reusability in Chip Design

**on Chip Owner**
- Application Specs
- Custom Domain IP

**on Design Platform**
- SoC Specs
- Architecture
- Key IP Configuration
- Verification Requirements
- HW/SW Bring-up
- Physical Implementation
- Physical Design
- PKG

Unique Value
Reusable Efforts
Platform-based AI Chip Development

NPU arch + SW stack

PLATFOrM

- SoC Arch.
- High-speed Interfaces
- Key IP Subblocks
- CPU coreplex
- Evaluation Board
- System SW Package
- Reusable Design Assets
- Ecosystem Enablement
- Supply Chain Mgmt
Our answer: Platform-based AI solution

**Lower Development Cost**
- Up to 50%+ lower* (vs industry average)
- Cost reduction for design NRE, Fabrication & IP licenses

**Rapid Time to Market**
- Up to 50%+ shorter* than industry average
- Maximize design / verification component reusability

**Reduced Engineering Risk**
- Pre-verified IPs and Silicon-proven Platform
- End-to-end solution with expertise from architecture consulting to PKG/Test/SW Bring-up

**Simplest Engagement Model**
- SEMIFIVE manages entire silicon design and manufacturing process (IP, EDA, Foundry, OSAT, etc)
- Customer can solely focus on their own technology/idea.

* Case with maximum reuse of SEMIFIVE’s platform SoC
Enabling innovators & disruptors to realize differentiated AI silicon

“Less than a week after the evaluation board was out, we were able to verify PCIe Gen5 and GDDR6 performance, thanks to SEMIFIVE. SEMIFIVE has really great S/W capabilities essential for Level 0 engagement. It was possible to submit MLPerf without a single package and board revision shows that SEMIFIVE has solid HW capabilities including PSI”

Source : Rebellions

Kick off to Tapeout in just 6 months!

Source : FuriosaAI
### AI Inference SoC platform 14nm

#### System Peripherals
- CPU
  - UART x2
- DDR3/4 LDDR
- 2MB L2CC

#### High Performance Interface
- PCIe Gen5 (x4/8/16)
- 2A DRAM
- LPDDR4 (x5-2GB)
- LPDDR4 (x5-4GB)
- LPDDR4 (x5-8GB)
- LPDDR4 (x5-16GB)

**Target market/application**
- Data center accelerator
- AI Vision processor
- Big data analytics
- Image/Video recognition
- ADAS with real time processing

**In mass production! 2 additional DWs using same platform**

### AIoT SoC platform 14nm

#### System Peripherals
- CPU
  - UART x2
- DDR3/4 LDDR
- 2MB L2CC

#### High Performance Interface
- PCIe Gen5 (x4)
- 2A DRAM
- LPDDR4 (x5-2GB)
- LPDDR4 (x5-4GB)
- LPDDR4 (x5-8GB)
- LPDDR4 (x5-16GB)

**Target market/application**
- Consumer (e.g., wearables)
- Surveillance and Smart Security
- Smart home
- Industrial IoT (incl smart factory)
- Robotics

**TO completed. Engaging multiple customers**

### HPC AI SoC platform 5nm

#### System Peripherals
- CPU
  - UART x2
- DDR3/4 LDDR
- 2MB L2CC

#### High Performance Interface
- PCIe Gen5 (x6/8/16)
- 2A DRAM
- LPDDR4 (x5-2GB)
- LPDDR4 (x5-4GB)
- LPDDR4 (x5-8GB)
- LPDDR4 (x5-16GB)

**Target market/application**
- Hyperscale Data Centers
- Cloud Servers
- Network Processors
- High performance AI accelerators

**First pass silicon success. 2nd TO completed in 1Q23**
### SEMIFIVE ASIC designs with other Tier1s / Set / OEMs companies

<table>
<thead>
<tr>
<th>Project</th>
<th>Application</th>
<th>Samsung Foundry Process node</th>
<th>Die Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>AI SoC</td>
<td>14nm</td>
<td>~ 200mm²</td>
</tr>
<tr>
<td>B</td>
<td>AI SoC</td>
<td>14nm</td>
<td>~ 200mm²</td>
</tr>
<tr>
<td>C</td>
<td>AI SoC</td>
<td>5nm</td>
<td>~ 150mm²</td>
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<tr>
<td>D</td>
<td>AI SoC</td>
<td>14nm</td>
<td>~ 200mm²</td>
</tr>
<tr>
<td>E</td>
<td>AI IOT</td>
<td>14nm</td>
<td>~ 80mm²</td>
</tr>
<tr>
<td>F</td>
<td>AI CV</td>
<td>8nm</td>
<td>~ 40mm²</td>
</tr>
<tr>
<td>G</td>
<td>5G Network</td>
<td>4nm</td>
<td>~ 300mm²</td>
</tr>
<tr>
<td>H</td>
<td>Energy SoC</td>
<td>4nm</td>
<td>~ 20mm²</td>
</tr>
</tbody>
</table>
SEMIFIVE – A little about us

**“New Global Hub of Custom Silicon”**

- Founded in 2019, completed 4 acquisitions*
- Engineering focused with 340+ Engineers
- USD$150M raised (up to Series B)
- Engineering team Experience - 250+ tapeouts
- SEMIFIVE has 10+ T/O on adv FinFET (14/8/5nm)
- Official Samsung Foundry SAFE DSP

* Sesol Semi, Dahsim Semi (2019), Hanatec (2021), AnalogBits (2022)

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**Flexible end2end turnkey ASIC service**

<table>
<thead>
<tr>
<th>Step</th>
<th>Image</th>
<th>Description</th>
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<tbody>
<tr>
<td>Idea hand-off</td>
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<td>Spec hand-off</td>
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<td>RTL hand-off</td>
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<td>Netlist hand-off</td>
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<td>GDSII hand-off</td>
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<td>SoC Specifications</td>
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<td>Top-level architecture</td>
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<td>IP integration</td>
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<td>Top-level verification</td>
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<td>Netlist synthesis</td>
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<td>Physical Design</td>
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<td>Tapeout/MPW/Flip</td>
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<td>Package Test</td>
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<td>SoC Bring-up</td>
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<td>Supply Chain Management</td>
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**Unique SOC Platforms**

**Rapid development enabled by**

- Domain Specific Architecture
- Pre-configured and verified IP pool
- Ready-to-action bring up HW/SW

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**We are global and growing**

- Engineers
  - S. Korea (HQ)
  - Vietnam
  - India
  - San Jose
  - 340+ 2023
  - 600+ 2025

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*Founded in 2019, completed 4 acquisitions*:

* Sesol Semi, Dahsim Semi (2019), Hanatec (2021), AnalogBits (2022)
Can I own my AI?

- Tremendous AI market and application opportunities
- More effort needed to address challenges in design architecture, memory optimization/options, latency, hybrid solutions etc
- We need tighter collaboration between idea creators, system innovators, chip designers, silicon providers to software teams

- And **YES!** You can own your AI with SEMIFIVE
THANK YOU

New Global Hub of Custom Silicon

More information can be found at our new website

www.semifive.com