YOUR IDEA TO SILICON

27 APR 2023
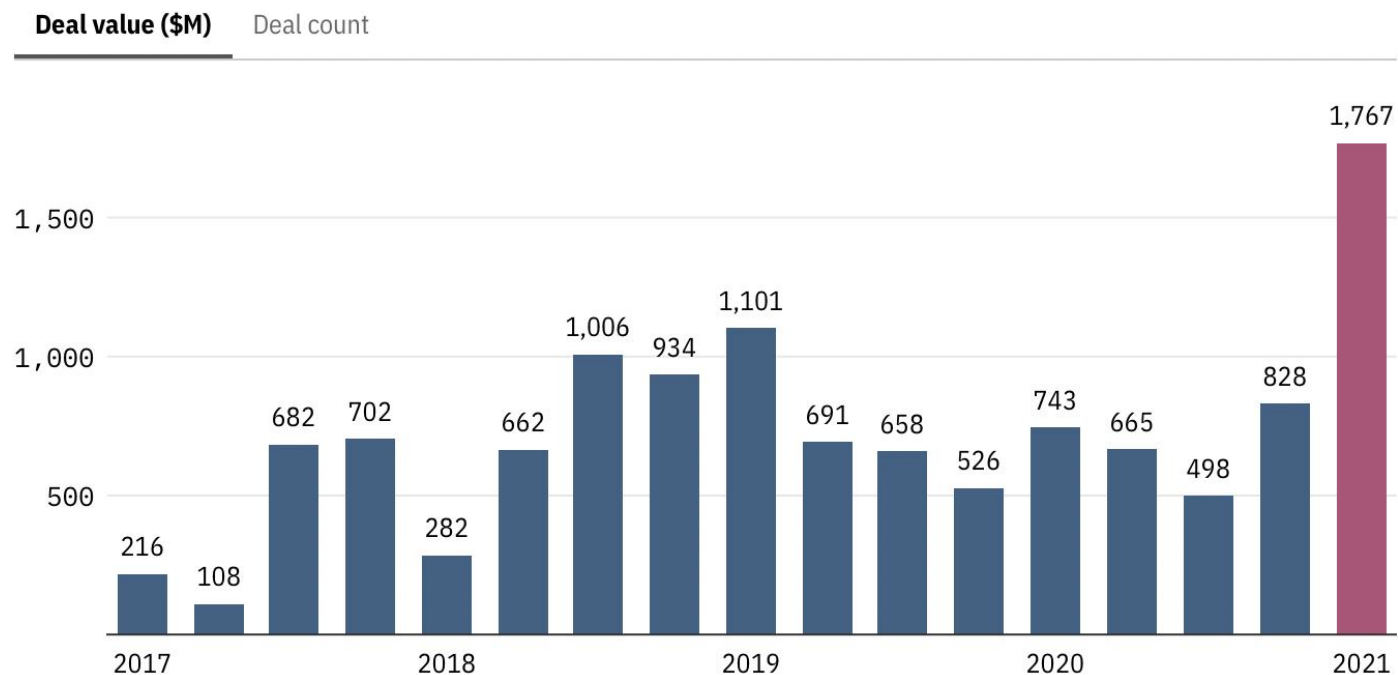
**Can I own my AI?**

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# AI semiconductor clearly sees a strong momentum

## AI and ML chip funding went through the roof in the first quarter of 2021
### Total VC spending on AI and ML semiconductors (2017-Q1 2021)

**Deal value ($M)**   Deal count



| Year | Value |
|------|-------|
| 2017 | 216 |
| 2017 | 108 |
| 2017 | 682 |
| 2017 | 702 |
| 2018 | 282 |
| 2018 | 662 |
| 2018 | 1,006 |
| 2019 | 934 |
| 2019 | 1,101 |
| 2019 | 691 |
| 2019 | 658 |
| 2020 | 526 |
| 2020 | 743 |
| 2020 | 665 |
| 2020 | 498 |
| 2021 | 828 |
| 2021 | 1,767 |

Source: PitchBook

**TECH**MONITOR

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AI chip technology is evolving rapidly, Gartner estimates that more than 50 companies are making chips specifically for AI, and **AI-specific chip revenue is expected to reach $76.8 billion by 2025**

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# Let's look at several key trends for AI SoCs

- **Accelerator-based designs**: <u>Domain Specific</u> IP for training and inference work <u>more efficiently</u> than general-purpose CPUs and GPUs.

- **AI at the Edge:** Growing trend towards processing AI workloads at the edge prioritize <u>low-power and smaller die size</u>

- **Memory Architecture:** <u>Reduced Latency</u> is the holy grail in AI workloads. Chip designs are increasingly focused on <u>optimizing memory architecture/choices</u>

- **Hybrid architectures:** Migration of AI chips using <u>combination of different types of accelerators</u> to optimize performance for specific AI workloads – <u>chiplet opportunity</u>

- **Increasing performance:** Demand for performance of AI chips (training), both in terms of die size, raw compute power and energy efficiency are driving innovation in chip design, materials science, and cooling technology.
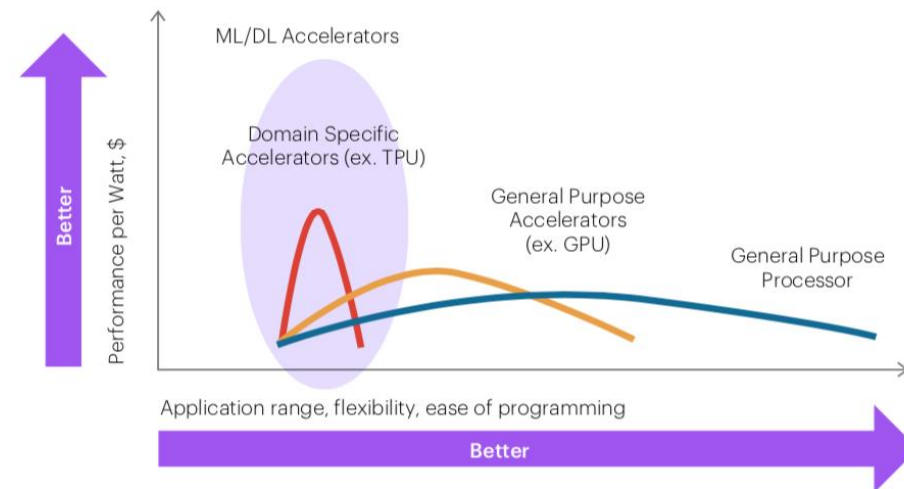


*Source : GSA AI whitepaper, Dell*

## Choosing the Correct Memory: Comparison Data

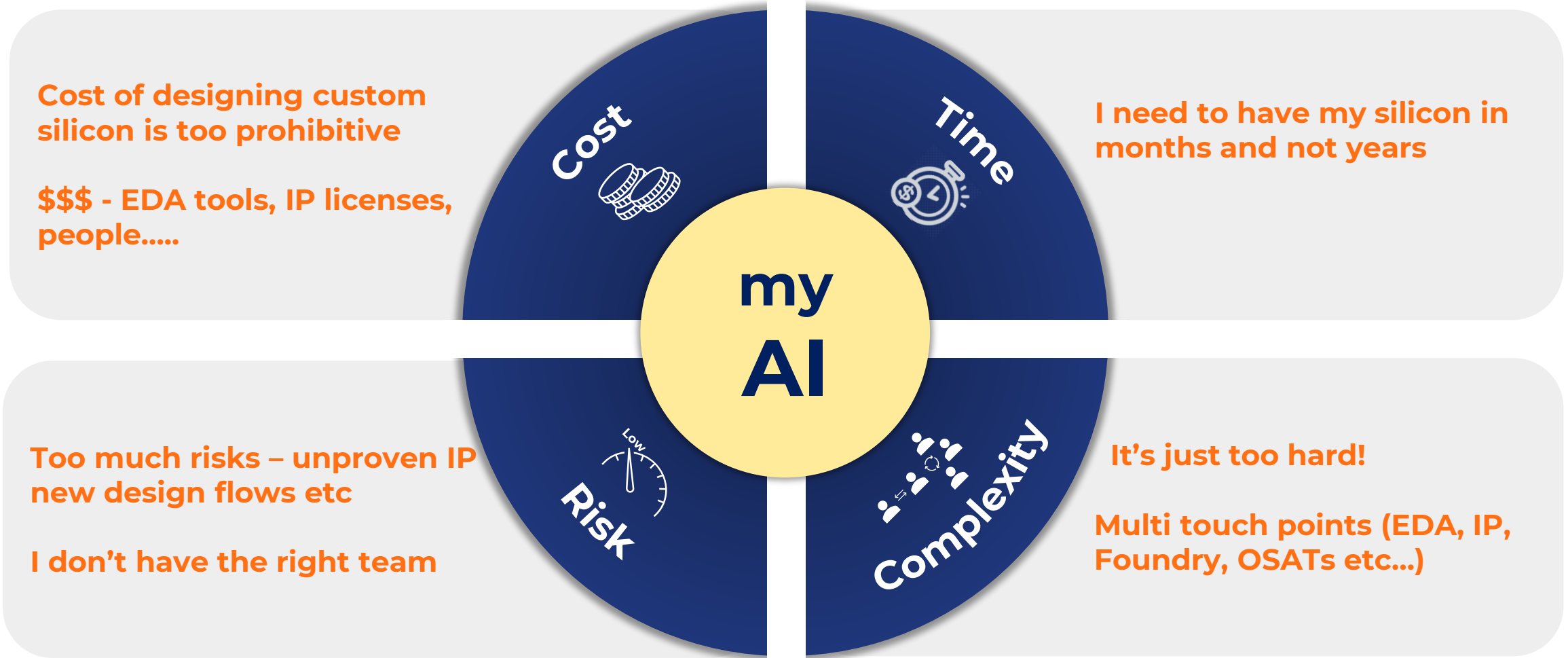| Parameter | LPDDR4x | LPDDR5 | DDR4 | GDDR6 | HBM2E |
|---|---|---|---|---|---|
| Bandwidth (Gbps) | Low-Medium (136) | Medium (204) | Medium (200) | High (512) | Highest (3686) |
| Data Rate (Gbps) | 4.266 | 6.4 | 3.2 | 16 | 3.6 |
| Interface width (bits) | 32 | 32 | 64 | 32 | 1024 |
| Board Area / System Design | Large / Medium | Medium/ Medium | Large / Easy | Medium / Medium | Small / Complex |
| Efficiency (mW/Gbps) | High (3) | High (3) | Moderate (10) | Moderate (10) | Highest (2) |
| Cost ($) | Medium | Medium | Low | Medium | High |
| Reliability/Yield | Good | Good | Good | Good | Moderate |
| Applications | Mobile, AI | Mobile, AI | Compute, Network | AI, Graphics, Auto | AI, HPC, Network |

*Source : Rambus*

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# *The AI Chip Revolution has begun.....*

*More effort and partnership collaboration is required to realize IDEAS and INNOVATION into Silicon*

**Cost of designing custom silicon is too prohibitive**

**$$$ - EDA tools, IP licenses, people.....**

**Cost**

**my AI**

**Time**

**I need to have my silicon in months and not years**

**Too much risks – unproven IP new design flows etc**

**I don't have the right team**

**Risk**

**Complexity**

**It's just too hard!**

**Multi touch points (EDA, IP, Foundry, OSATs etc...)**
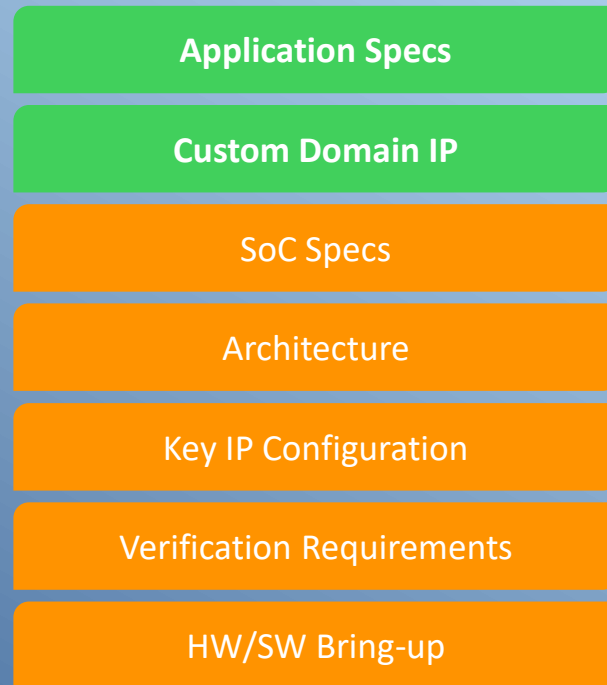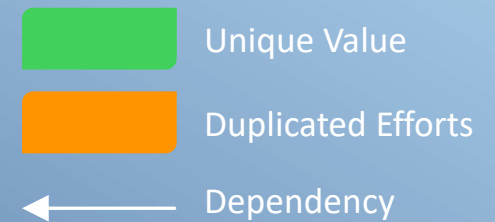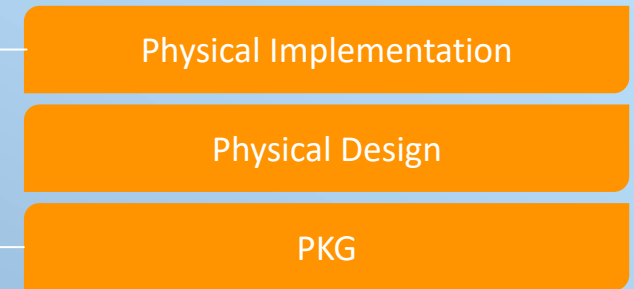
**Need to Dramatically Enhance Design Reusability in Chip Design**

## on Chip Owner

| Application Specs |
|---|

| Custom Domain IP |
|---|

■ Unique Value

■ Reusable Efforts

## on Design Platform

| SoC Specs |
|---|

| Architecture |
|---|

| Key IP Configuration |
|---|

| Verification Requirements |
|---|

| HW/SW Bring-up |
|---|

| Physical Implementation |
|---|

| Physical Design |
|---|

| PKG |
|---|

**Platform-based AI Chip Development**

NPU arch + SW stack

+

## PLATFORM

| SoC Arch. | High-speed Interfaces | Key IP Subblocks |
| --- | --- | --- |
| CPU coreplex | Evaluation Board | System SW Package |
| Reusable Design Assets | Ecosystem Enablement | Supply Chain Mgmt |

# Our answer : Platform-based AI solution

## Lower Development Cost

- **Up to 50%+ lower*** (vs industry average)
- Cost reduction for design NRE, Fabrication & IP licenses

## Rapid Time to Market

- **Up to 50%+ shorter*** than industry average
- Maximize design / verification component reusability

**Cost**

**Time**

**SEMIFIVE Design Platform**

**Risk**

**Complexity**

## Reduced Engineering Risk

- Pre-verified IPs and Silicon-proven Platform
- End-to-end solution with expertise from architecture consulting to PKG/Test/SW Bring-up

## Simplest Engagement Model

- SEMIFIVE manages entire silicon design and manufacturing process (IP, EDA, Foundry, OSAT, etc)
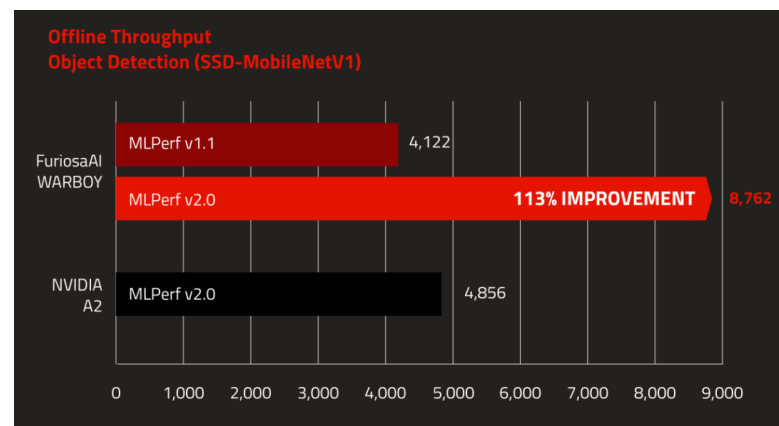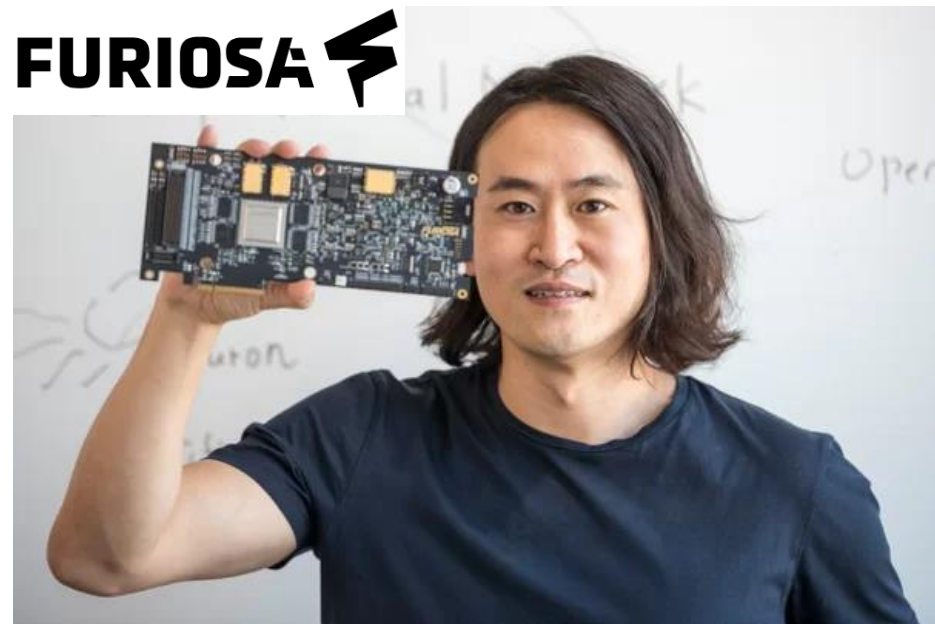- Customer can solely focus on their own technology/idea.

*\* Case with maximum reuse of SEMIFIVE's platform SoC*

# Enabling innovators & disruptors to realize differentiated AI silicon



"Less than a week after the evaluation board was out, we were able to verify PCIe Gen5 and GDDR6 performance, thanks to SEMIFIVE. SEMIFIVE has really great S/W capabilities essential for Level 0 engagement. It was possible to submit MLPerf without a single package and board revision shows that SEMIFIVE has solid HW capabilities including PSI"
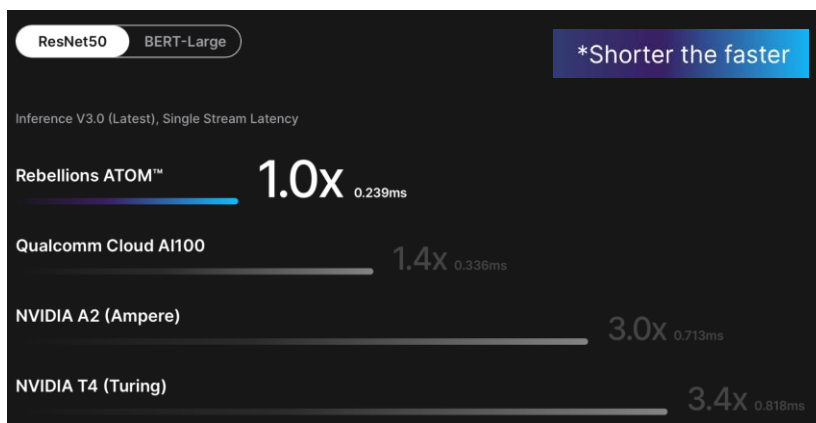


Source : Rebellions



Source : FuriosaAI



Kick off to Tapeout in just
**6 months!**

# Examples: Platform-based AI chips taped out at Samsung Foundry



| AI Inference SoC platform 14nm | AIoT SoC platform 14nm | HPC AI SoC platform 5nm |
|---|---|---|

**Target market/application**
- Data center accelerator
- AI Vision processor
- Big data analytics
- Image/Video recognition
- ADAS with real time processing

*In mass production! 2 additional DWs using same platform*

**Target market/application**
- Consumer (e.g., wearables)
- Surveillance and Smart Security
- Smart home
- Industrial IoT (incl smart factory)
- Robotics

*TO completed. Engaging multiple customers*

**Target market/application**
- Hyperscale Data Centers
- Cloud Servers
- Network Processors
- High performance AI accelerators

*First pass silicon success. 2nd TO completed in 1Q23*

# SEMIFIVE ASIC designs with other Tier1s / Set / OEMs companies

| Project | Application | Samsung Foundry Process node | Die Size |
|---------|-------------|------------------------------|----------|
| A | AI SoC | 14nm | ~ 200mm$^2$ |
| B | AI SoC | 14nm | ~ 200mm$^2$ |
| C | AI SoC | 5nm | ~ 150mm$^2$ |
| D | AI SoC | 14nm | ~ 200mm$^2$ |
| E | AI IOT | 14nm | ~ 80mm$^2$ |
| F | AI CV | 8nm | ~ 40mm$^2$ |
| G | 5G Network | 4nm | ~ 300mm$^2$ |
| H | Energy SoC | 4nm | ~ 20mm$^2$ |

# SEMIFIVE – A little about us

## "New Global Hub of Custom Silicon"

- Founded in 2019, completed 4 acquisitions*
- Engineering focused with 340+ Engineers
- USD$150M raised (up to Series B)
- Engineering team Experience - 250+ tapeouts
- SEMIFIVE has 10+ T/O on adv FinFET (14/8/5nm)
- Official Samsung Foundry SAFE DSP
  *Sesol Semi, Dahsim Semi (2019), Hanatec (2021), AnalogBits (2022)*
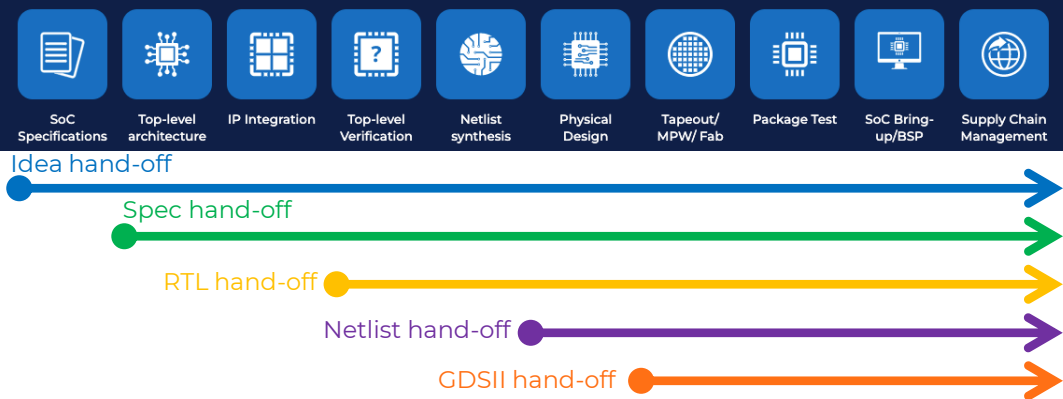
## We are global and growing

India

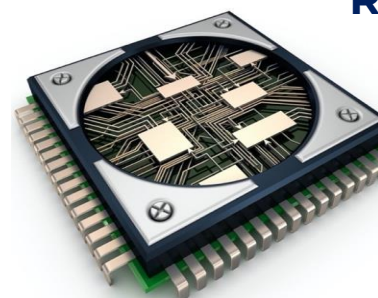S. Korea (HQ)

Vietnam

ANALOG BITS
San Jose

Engineers

**340+** 2023

**600+** 2025

## Flexible end2end turnkey ASIC service

| SoC Specifications | Top-level architecture | IP Integration | Top-level Verification | Netlist synthesis | Physical Design | Tapeout/ MPW/ Fab | Package Test | SoC Bring-up/BSP | Supply Chain Management |
|---|---|---|---|---|---|---|---|---|---|

Idea hand-off

Spec hand-off

RTL hand-off

Netlist hand-off

GDSII hand-off

## Unique SOC Platforms

### Rapid development enabled by

Domain Specific Architecture

Pre-configured and verified IP pool

Ready-to-action bring up HW/SW

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# Can I own my AI?

❑ Tremendous AI market and application opportunities

❑ More effort needed to address challenges in design architecture, memory optimization/options, latency, hybrid solutions etc

❑ We need tighter collaboration between idea creators, system innovators, chip designers, silicon providers to software teams

❑ And **YES!** **You can own your AI with SEMIFIVE**

SAFE™-DSP
Design Solution Partner

SEMI FIVE

SAMSUNG FOUNDRY

# THANK YOU

**New Global Hub of Custom Silicon**

*More information can be found at our new website*

*www.semifive.com*