Multi-Die Systems: The Future of Semiconductors

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Synopsys Enables System Innovation, Silicon to Software

Comprehensive World-Class Technology

Software:
Application security & quality testing, Leader in Gartner’s Magic Quadrant

Systems:
Leader in HW/SW verification, virtual prototyping, VIP and models

Design:
Digital & custom AMS families
Best QoR, highest productivity

IP:
Broadest portfolio, silicon-proven
#1 in interface, foundation & physical IP

Silicon:
Reference tools for process optimization, CAD, lithography & yield optimization

Solutions:
Multi-die, Automotive, low power, DTCO, memory, SLM, optics, photonic IC

PROCESS FUNDAMENTALS

Brodest System Design Coverage

DEPLOYED SYSTEM
Semiconductor Design Productivity Waves

Multi-die system: A key enabler of the SysMoore era

- Circuit Simulation
- Layout & Place & Route
- Digital Simulation & Synthesis
- IP Reuse
- Multi-Die Systems

Log Complexity

Key Drivers of This New Wave: The Many Walls

- The "Processing Wall"
- The "Memory Wall"
- The "Connectivity Wall"
Key Drivers of This New Wave: Plus, the Limits of 2D Scaling

Density-Scaling Slowing

Increasing Costs

... Leading to Increasing Demand for Multi-Die Systems
The Shift to Multi-Die Systems

Motivation for Multi-Die Systems

- Accelerated scaling of system functionality at a cost-effective price (>2X reticle limits)
- Reduced risk & time-to-market by re-using proven designs/die
- Lower system power while increasing throughput (up to 30%)

From System-on-Chip to System-of-Chips
The SysMoore Era of Multi-Die System is Here

Synopsys Tracking >100 Multi-Die System Designs

- Servers / AI dominate
- NICs, Switches common use case
- Smartphone / Graphics / PC primarily proprietary
- Co-packaged Optics, Automotive ramping
Bringing New Challenges and Opportunities...

“Silicon-Out” Disruption

Automotive, Mobile
Architectural Design
Innovation

HPC
Native System Analysis
(Power/Thermal...)
(10s to 100+)

HPC
Native Integration
Verify Productivity
constraints for design/verification

HPC
Native System Analysis
(System Lifecycle
Health)

Mobile Infrastructure
Package Innovation

HPC
Scale Innovation
Bump Pitch, 3D P&R

Heterogeneous
Integration
(also for 6G, Photonics...)

Networking
UCIe/HBMx IP
Optimized Solution
and auto-routing

Image Sensor
Native Integration
Exploit scalability and
implementations of millions
of bump connections

Native System Analysis
(Power/Thermal,...), fast ECO

Foundry, Hyperscaler
Ensure multi-
die quality, yield
and system robustness

PLANNING/VERIFY

HPC
Ensure multi-
die System Lifecycle
Health

APPLICATION

COMPLEXITY

AUTOMATION

Native Integration
Verify Productivity

Automotive, Mobile
Architectural Design
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COMPLEXITY

AUTOMATION
Synopsys Multi-Die System Solution
A comprehensive solution for heterogeneous integration

Architecture Exploration
- Optimize thermal, power, and performance with early exploration and partitioning

Software Dev. & Validation
- Rapid software development and validation with high-capacity emulation & prototyping

Design Implementation
- Efficient die/package co-design with unified exploration-to-signoff platform and robust IP

Manufacturing & Reliability
- Improve health, security and reliability with holistic test and lifecycle management solutions
Early Architecture Exploration For Multi-Die Systems

Optimize performance, power & thermal KPIs with platform architect

<table>
<thead>
<tr>
<th>PARTITION INTO DIES/CHIPLETS</th>
<th>OPTIMIZE MULTI-DIE SYSTEM</th>
<th>ACCELERATE ARCHITECTURE REALIZATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Separate system into its functions, scale functions across multiple dies</td>
<td>Optimize for bandwidth density, energy per bit, cost and latency</td>
<td>Enable silicon, package and software teams with multi-die system model</td>
</tr>
<tr>
<td>Meet scaling, fabrication, and functionality requirements</td>
<td>Select chip-to-chip protocols and interfaces: UCIe, PCIe, CXL, …</td>
<td>Leverage die-on-die and die-to-die IP/VIP models</td>
</tr>
</tbody>
</table>

Scalable Design Space Exploration

Model-Based Architectural Exploration of Multi-die Systems

- CPU 32
- CPU 64
- GPU
- AI
- …
Software Development & System Validation

Fast, high-capacity virtual, emulation and prototyping engines

**FAST SOFTWARE BRING-UP**
Early chiplet virtual models for software teams

**SCALE COMPLEXITY**
Best multi-die system scalability for 30B gates

**OPTIMIZE VALIDATION CYCLE**
Minimize bring-up time with proven models, transactors, speed adapters

Multiple Heterogeneous Pre-silicon Platforms

- Virtual Prototyping
  - Virtual Prototype Virtualizer
  - Virtual Interface ZeBu Transactor
- Hybrid with ZeBu
  - Emulation ZeBu
- Hardware-Assisted Verification
  - Prototype HAPS
  - Emulation ZeBu
  - Die Board
Robust and Secure IP at the Heart of Multi-Die Systems

Synopsys UCIe Die-to-Die IP: Complete solution based on silicon-proven technology

Multi-Die System

Controller
- Interface Bridge (CXS/AXI)
- D2D Adapter
- PHY
- Test & Diagnostics
- Verification IP
- SiPi
- Subsystems

Advanced/Standard Packages

UCIe Controller IP
- Low latency bridge for NoCs in a multi-die system
- Optional security engine with encryption

UCIe PHY IP
- Low latency & power for interposer & substrate designs
- Extensive test & debug features for KGD

UCIe Verification IP
- Scalable architecture to support verification of various DUT types
- Build-in protocol checks and functional coverages at all layers
Synopsys IP Chiplets for Multi-Die Systems

**BROAD IP PORTFOLIO**
- Foundation IP
- Interface IP
- Security IP
- Processor IP

**IP SUBSYSTEMS**
Configured Interfaces (i.e., PCIe Subsystem)
- Silicon proven
- High quality
- Secure
- Pre-validated
- Integration-ready

**IP CHIPLETS**
- Ethernet IO Chiplet
- Memory Expander Chiplet
- AI Accelerator Chiplet

- Built on Synopsys’ silicon-proven, high-quality IP portfolio
- Flexibility to support multiple package types
- Customizable to target application
- Key features
  - Standards-compliant interfaces
  - Hierarchical test
  - Built-in security
  - Silicon lifecycle management
  - Yield enhancement functionality
Unified Co-Design Environment for Multi-Die Systems

Synopsys 3DIC Compiler: Industry’s only integrated co-design and analysis solution

- **System Architecture & Planning**
  - Common Fusion Data-model

- **Exploration & Creation**
- **Implementation**
- **System Signoff**

- **Multi-Die System**

- **Highly Integrated, Scalable Platform**
  - **Heterogenous integration** of 100s of billions of transistors
  - Billion+ inter-connections in a few hours

- **Seamless 2D to 3D Design Continuity**
  - Common data-model and tech-files
  - Efficient, concurrent workflow for faster closure

- **Unified Full-Flow Productivity**
  - Single environment, GUI and netlist for full system design
  - Full breadth of integrated engines: design, test, analysis, verification

- **Trusted, Golden-Signoff Analysis**
  - Industry standard technologies – STA, Thermal, EMIR, SI/PI
  - Fast convergence to optimal PPA/mm³, accelerate tapeout
Enable A Seamless Architecture-to-Design-to-Signoff Journey

Create, implement, refine, converge

**ARCHITECTURE DEFINITION**
- Functional Requirements
- Constraints: Performance, power, aspects, die/mm², Thermal
- Functions:
  - Chipset
  - Memory
  - SRAM
  - DRAM
  - FRAM
  - RRAM
  - MRAM
  - Package

**PARTITIONING AND TECHNOLOGY SELECTION**

**MULTI-DIE SYSTEM PROTOTYPING / 3D FLOORPLANNING**
- 3D FLOORPLAN

**MULTI-DIE SYSTEM HETEROGENEOUS DESIGN, 3D DESIGN IMPLEMENTATION**
- 3D IMPLEMENTATION (INC. TEST)

**MULTI-DIE SYSTEM FUNCTIONAL VERIFICATION**
- Function
  - Bandwidth
  - Throughput
  - Latency
  - ...

**MULTI-DIE SYSTEM SIGNOFF ANALYSIS**
- Timing
  - Power
  - Thermal
  - SI/PI
  - EMIR
  - DRC/LVS
  - ...

**ANALYSIS-DRIVEN EXPLORATION AND DESIGN**
Manufacturing Ramp and Product Reliability

**Multi-Die System Test & Repair**
Product Quality (KGD, Package, System)

- Ensure quality with comprehensive test, debug, repair for multi-die systems
- Integrated Test for: Multiple Dies, Memories, Interconnects, and Full-system

**Silicon Lifecycle Management**
Reliability, Yield, Health

- Enhance multi-die system operational metrics through environmental, structural, functional monitoring
- Solution Comprises: Silicon IP, EDA Software, and Analytics Insights

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<th>In-Design</th>
<th>In-Ramp</th>
<th>In-Production</th>
<th>In-Field</th>
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<tr>
<td>Power/Performance Optimization</td>
<td>Yield, Failure Analysis</td>
<td>Volume Test, Quality and Traceability</td>
<td>Optimization, Safety, Security, Maintenance</td>
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**Test Access**
IEEE 1838

**Logic-to-Logic**
PHY Monitor, Test & Repair

**Logic-to-Memory**
Ext. Memory BIST & Repair

**Via / Bump / Interconnect**
High volume Lane Test & Repair

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Summary: Multi-Die Systems – Future of Semiconductors

- Billion-Scale 3D Systems
- Heterogeneous Integration
- Advanced Packaging

Industry-wide collaborations to catalyze SysMoore Era innovations
Thank You