SYNOPSYS®

Multi-Die Systems: The Future of Semiconductors

GSA TECHNOLOGY SYMPOSIUM

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Shekhar Kapoor
Sr. Product Line Director

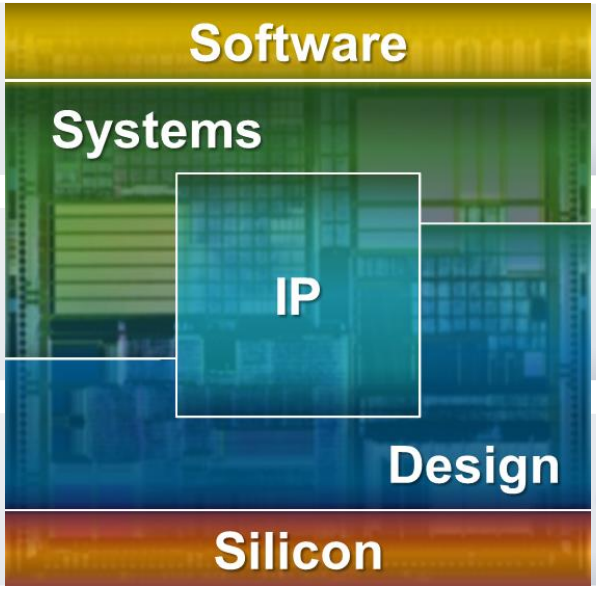
Synopsys Enables System Innovation, Silicon to Software

Comprehensive World-Class Technology

Software:
Application security & quality testing,
Leader in Gartner's Magic Quadrant

Systems:
Leader in HW/SW verification, virtual prototyping, VIP and models

Design:
Digital & custom AMS families
Best QoR, highest productivity



IP:
Broadest portfolio, silicon-proven
#1 in interface, foundation & physical IP

Silicon:
Reference tools for process optimization, CAD, lithography & yield optimization

Solutions:
Multi-die, Automotive, low power, DTCO, memory, SLM, optics, photonic IC

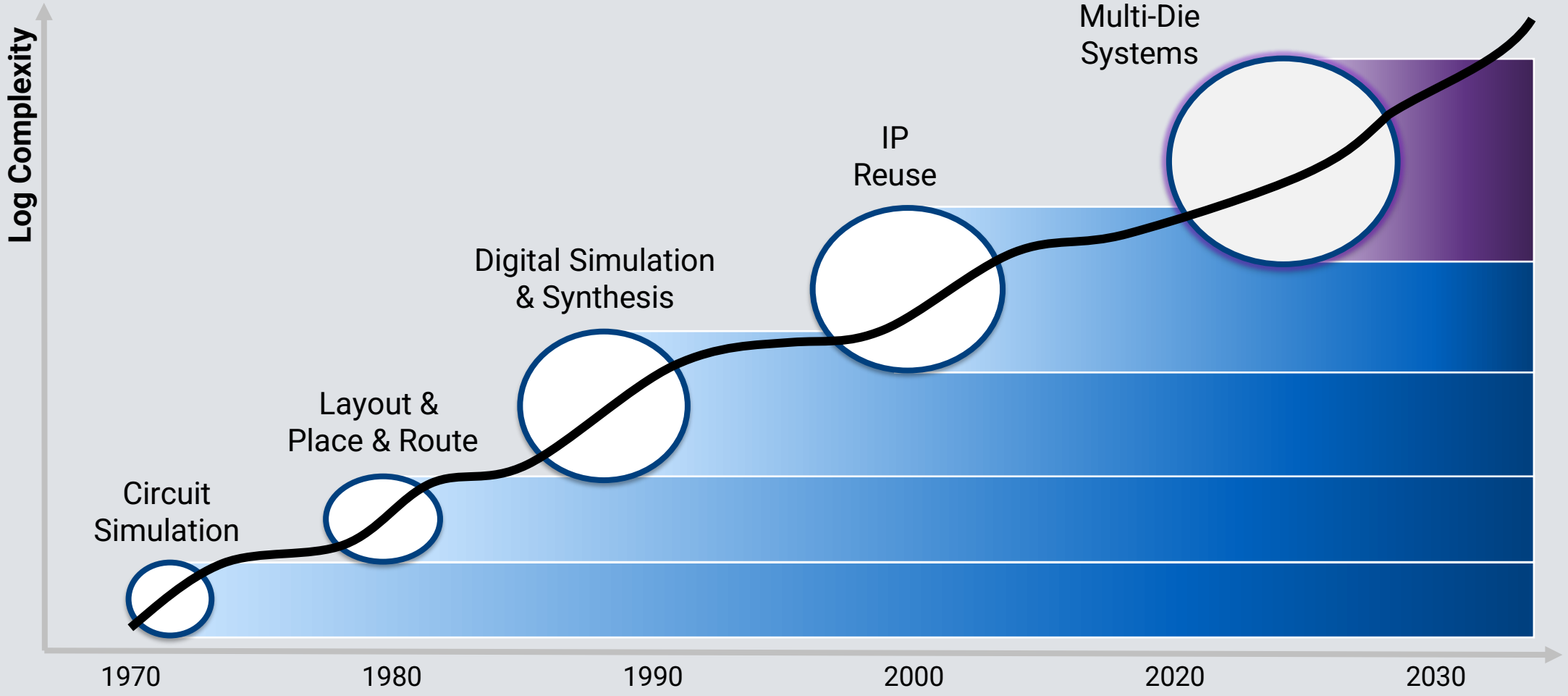
PROCESS FUNDAMENTALS

Broadest System Design Coverage

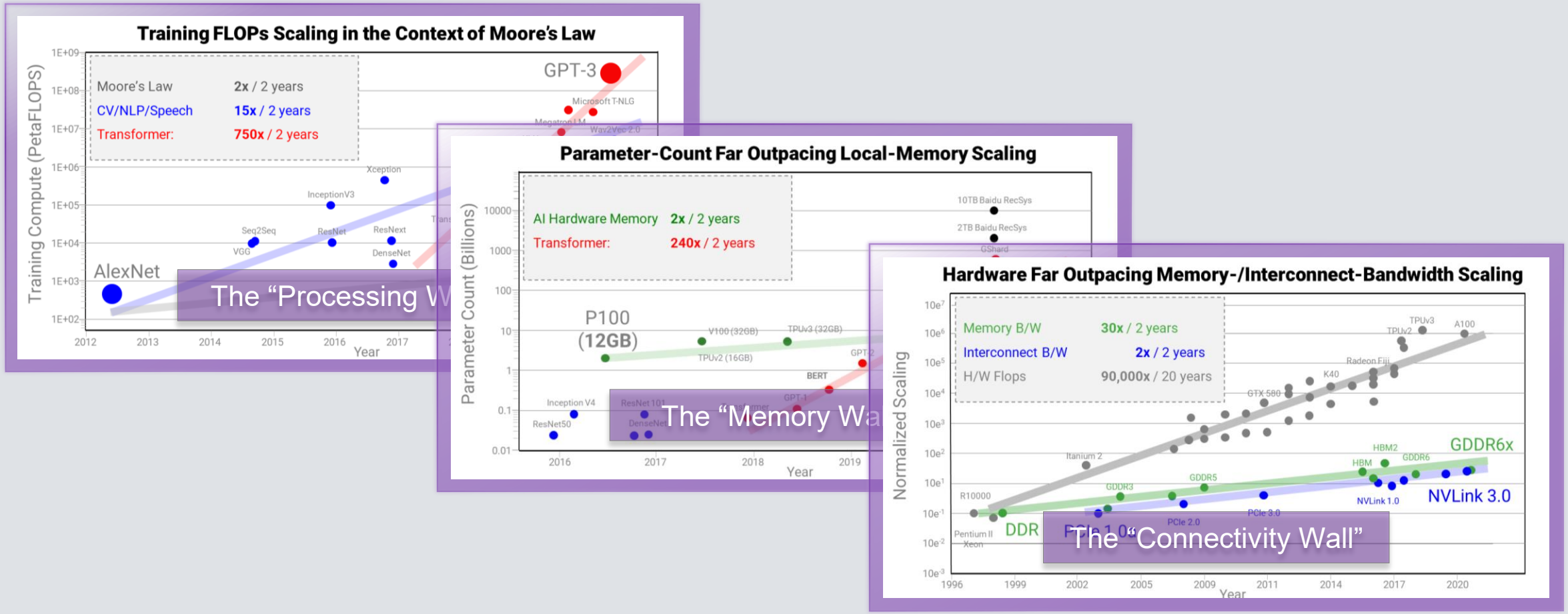
DEPLOYED SYSTEM

Semiconductor Design Productivity Waves

Multi-die system: A key enabler of the SysMoore era

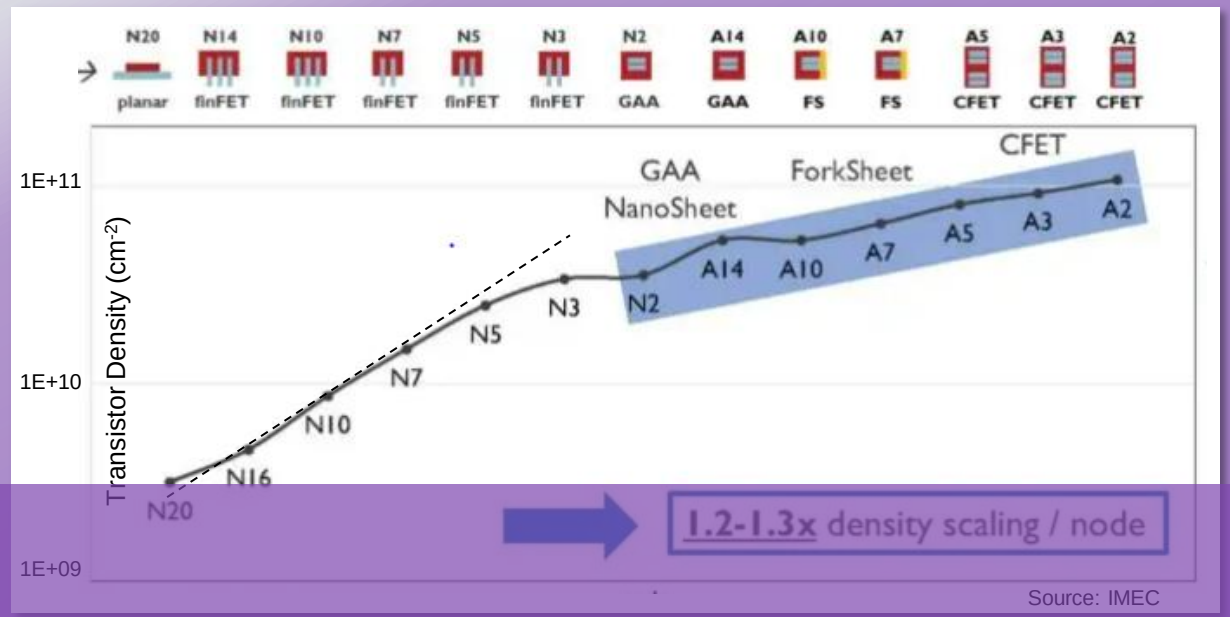


Key Drivers of This New Wave: The Many Walls



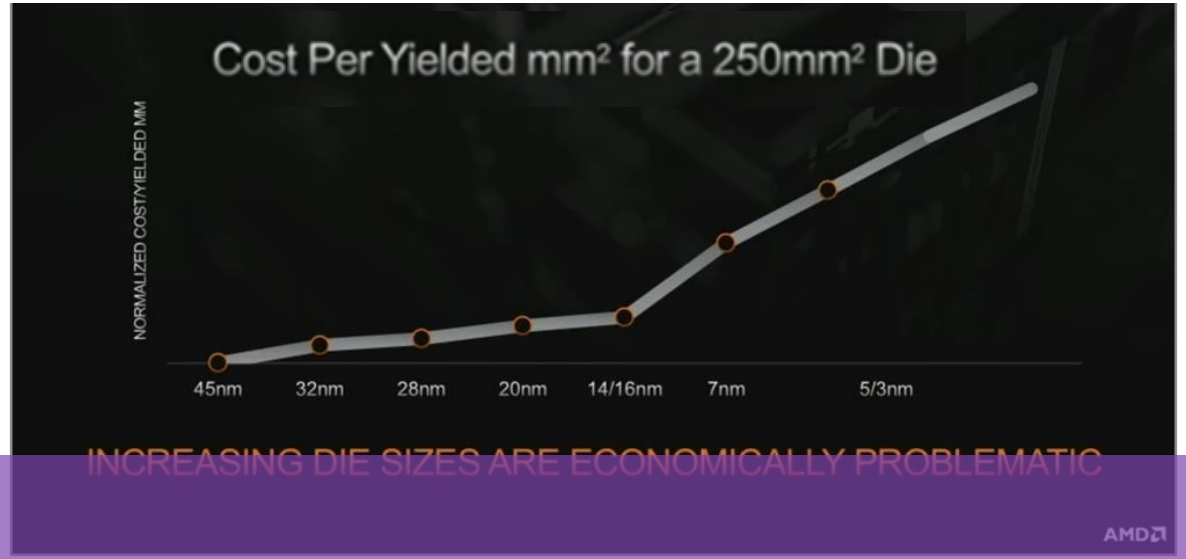
Key Drivers of This New Wave: Plus, the Limits of 2D Scaling

Density-Scaling Slowing



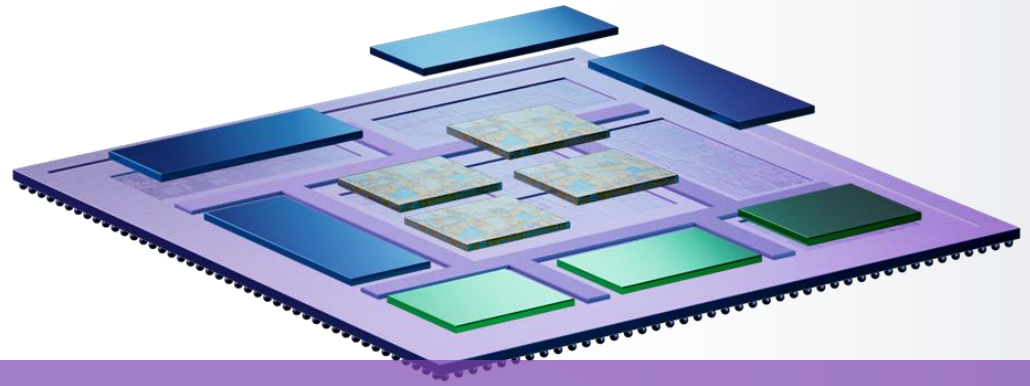
Source: IMEC

Increasing Costs



… Leading to Increasing Demand for Multi-Die Systems

The Shift to Multi-Die Systems



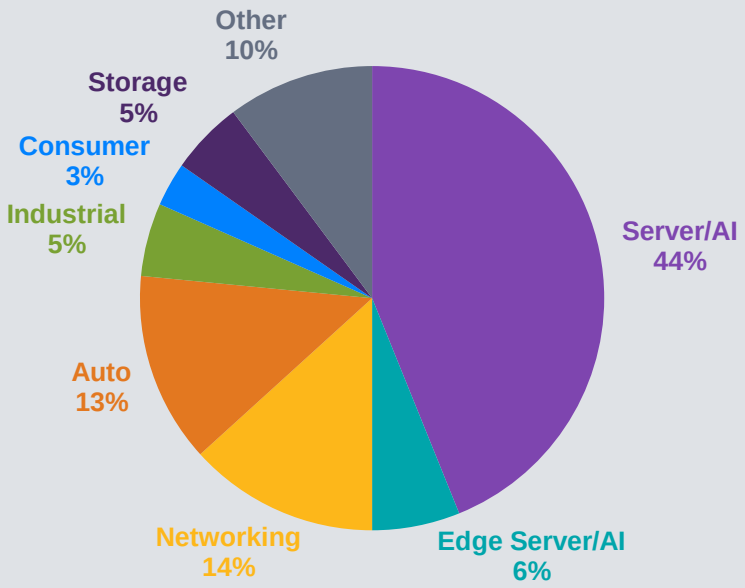
Motivation for Multi-Die Systems

- Accelerated scaling of system functionality at a cost-effective price (>2X reticle limits)
- Reduced risk & time-to-market by re-using proven designs/die
- Lower system power while increasing throughput (up to 30%)
- Rapid creation of new product variants for flexible portfolio management

From System-on-Chip to System-of-Chips

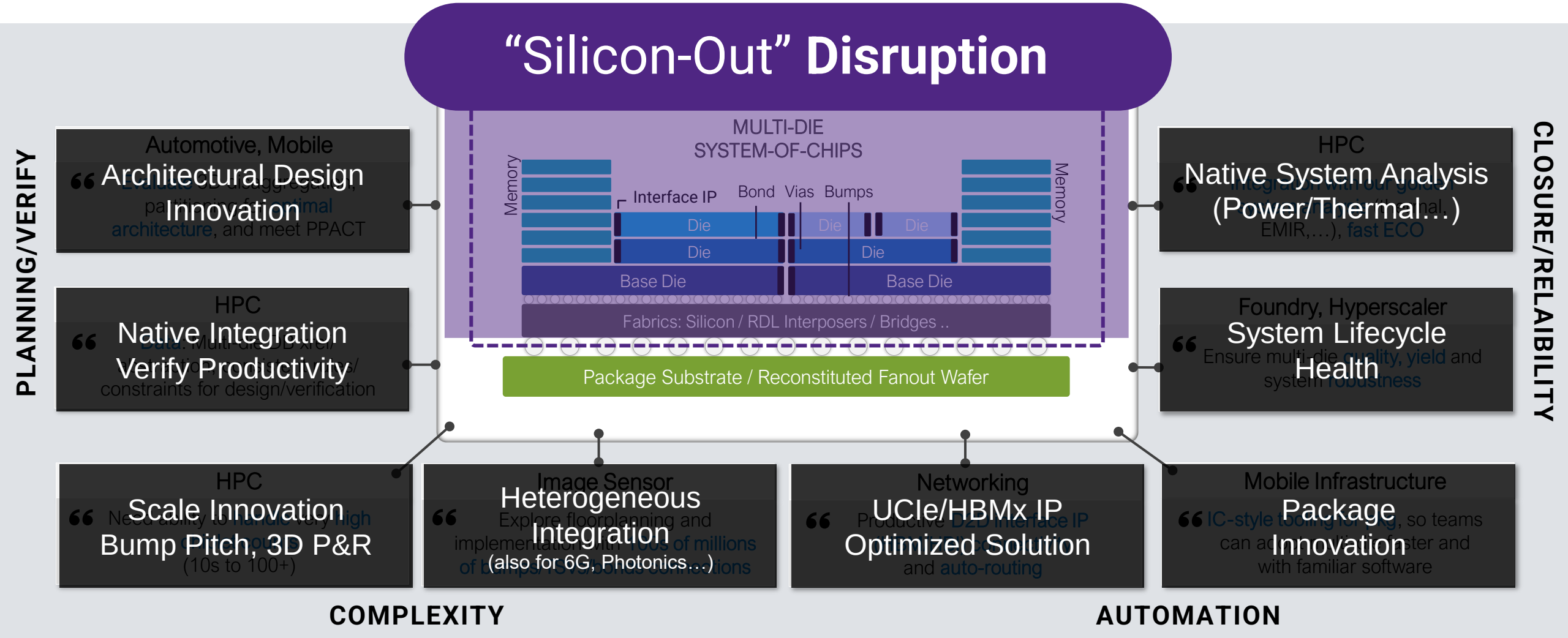
The SysMoore Era of Multi-Die System is Here

Synopsys Tracking >100 Multi-Die System Designs



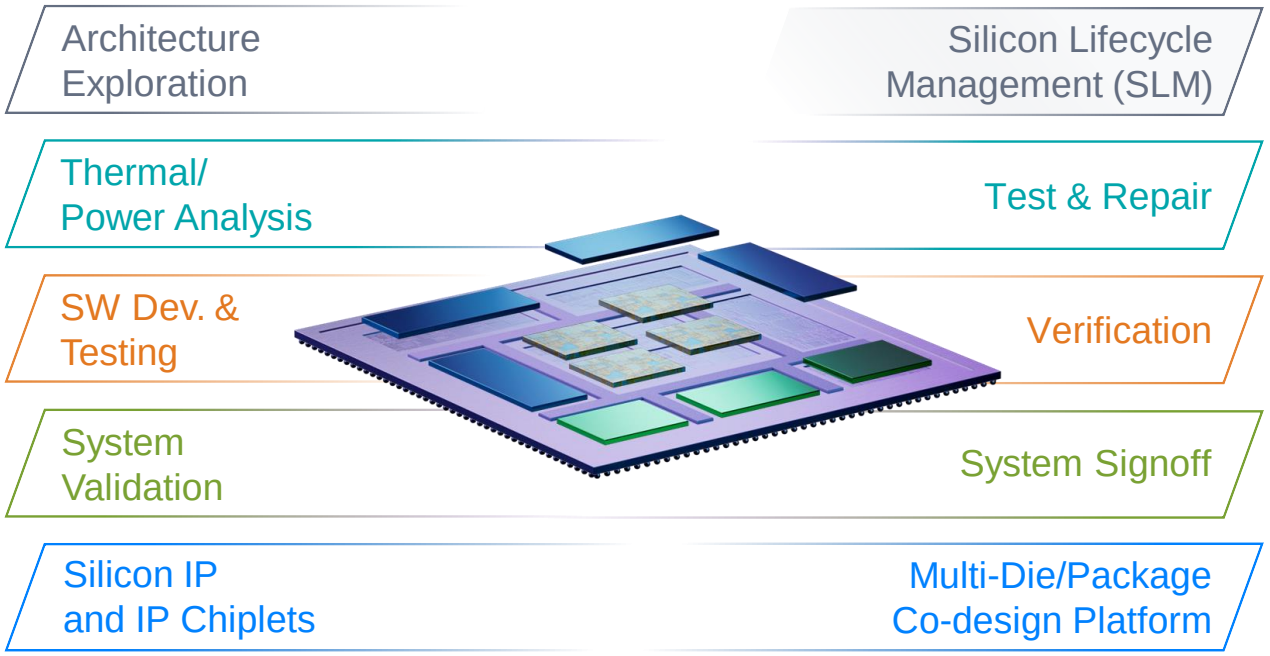
- Servers / AI dominate
- NICs, Switches common use case
- Smartphone / Graphics / PC primarily proprietary
- Co-packaged Optics, Automotive ramping

Bringing New Challenges and Opportunities…



Synopsys Multi-Die System Solution

A comprehensive solution for heterogeneous integration

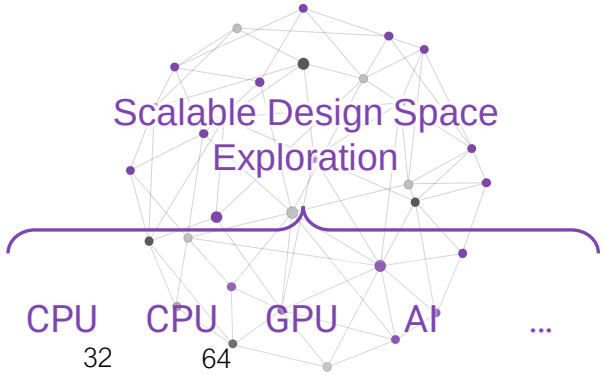


Architecture Exploration	Optimize thermal, power, and performance with early exploration and partitioning
Software Dev. & Validation	Rapid software development and validation with high-capacity emulation & prototyping
Design Implementation	Efficient die/package co-design with unified exploration-to-signoff platform and robust IP
Manufacturing & Reliability	Improve health, security and reliability with holistic test and lifecycle management solutions

Early Architecture Exploration For Multi-Die Systems

Optimize performance, power & thermal KPIs with platform architect

PARTITION INTO DIES/CHIPLETS

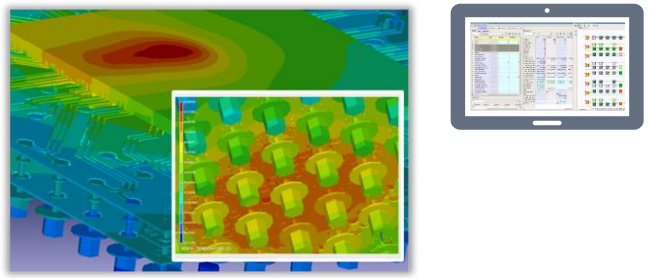


Separate system into its functions, scale functions across multiple dies

Meet scaling, fabrication, and functionality requirements

OPTIMIZE MULTI-DIE SYSTEM

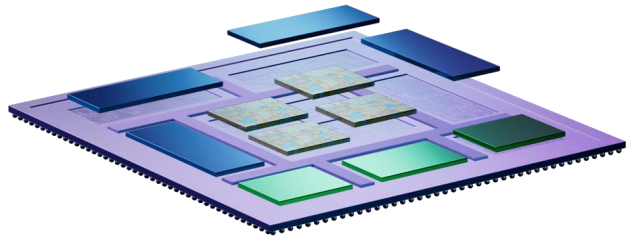
Model-Based Architectural Exploration of Multi-die Systems



Optimize for bandwidth density, energy per bit, cost and latency

Select chip-to-chip protocols and interfaces: UCIe, PCIe, CXL, …

ACCELERATE ARCHITECTURE REALIZATION



Enable silicon, package and software teams with multi-die system model

Leverage die-on-die and die-to-die IP/VIP models

Software Development & System Validation

Fast, high-capacity virtual, emulation and prototyping engines

FAST SOFTWARE BRING-UP

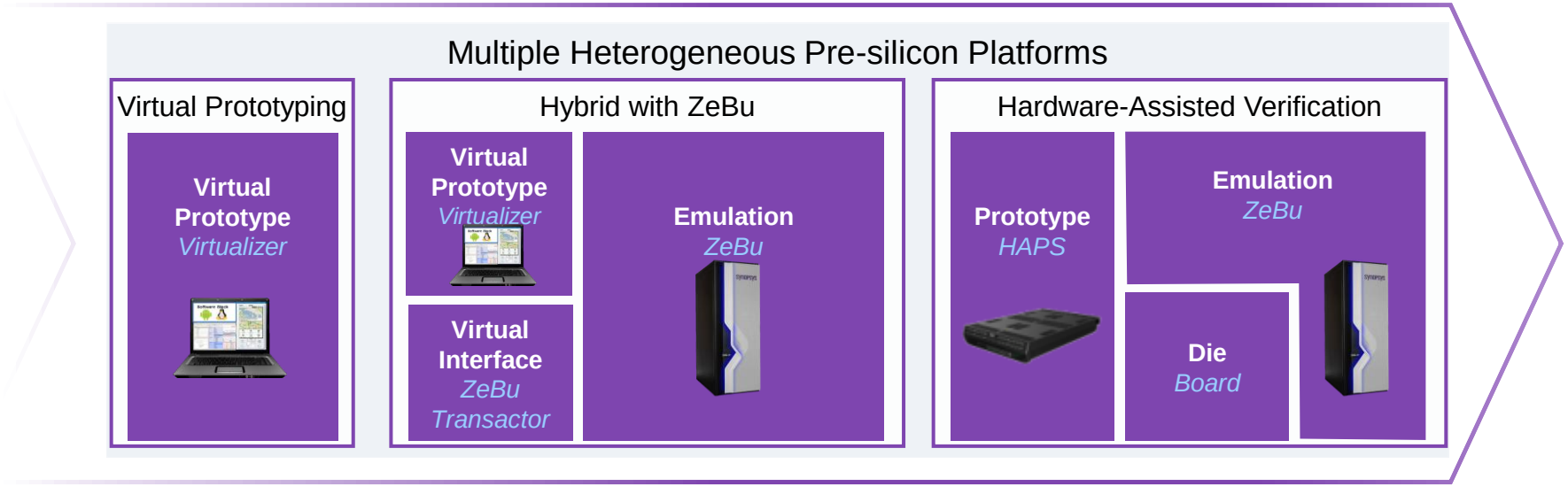
Early chiplet virtual models for software teams

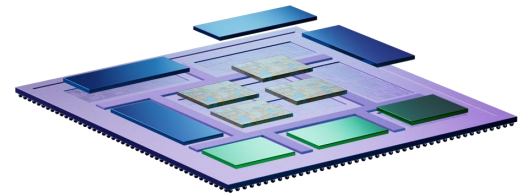
SCALE COMPLEXITY

Best multi-die system scalability for 30B gates

OPTIMIZE VALIDATION CYCLE

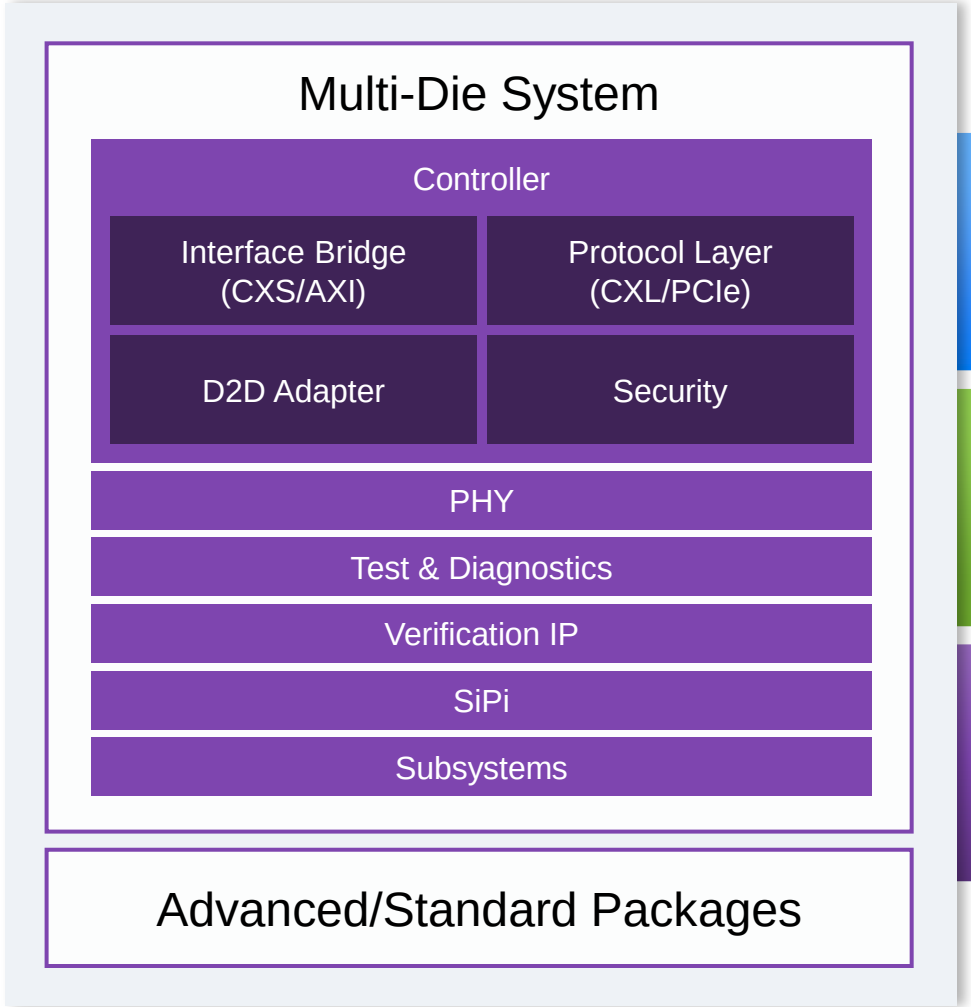
Minimize bring-up time with proven models, transactors, speed adapters





Robust and Secure IP at the Heart of Multi-Die Systems

Synopsys UCIe Die-to-Die IP: Complete solution based on silicon-proven technology



UCIe Controller IP

Low latency bridge for NoCs in a multi-die system

Optional security engine with encryption

UCIe PHY IP

Low latency & power for interposer & substrate designs

Extensive test & debug features for KGD

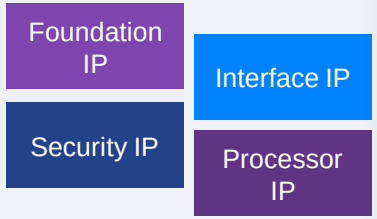
UCIe Verification IP

Scalable architecture to support verification of various DUT types

Build-in protocol checks and functional coverages at all layers

Synopsys IP Chiplets for Multi-Die Systems

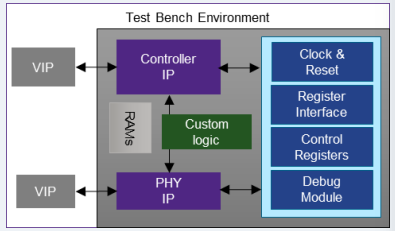
BROAD IP PORTFOLIO



- Silicon proven
- High quality
- Secure

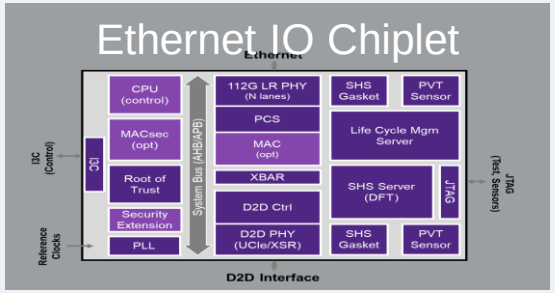
IP SUBSYSTEMS

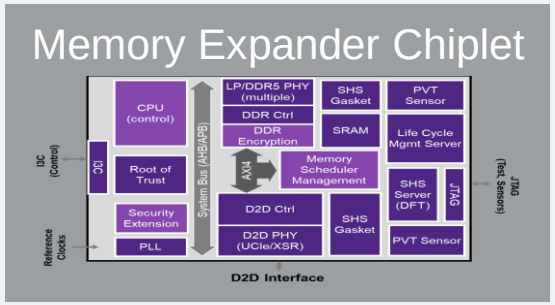
Configured Interfaces (ie, PCIe Subsystem)

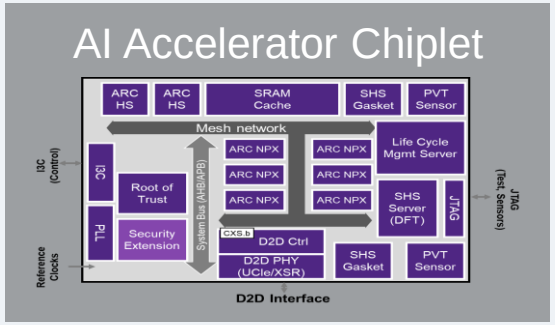


- Pre-validated
- Integration-ready

IP CHIPLETS







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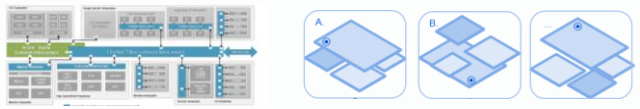
- Built on Synopsys' silicon-proven, high-quality IP portfolio
- Flexibility to support multiple package types
- Customizable to target application
- Key features
  - Standards-compliant interfaces
  - Hierarchical test
  - Built-in security
  - Silicon lifecycle management
  - Yield enhancement functionality

Unified Co-Design Environment for Multi-Die Systems

Synopsys 3DIC Compiler: Industry's only integrated co-design and analysis solution

System Architecture & Planning



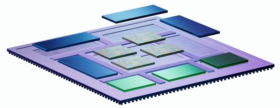
Exploration & Creation

Implementation

System Signoff

Common Fusion Data-model

Multi-Die System



Highly Integrated, Scalable Platform

Heterogenous integration of 100s of billions of transistors

Billion+ inter-connections in a few hours

Seamless 2D to 3D Design Continuity

Common data-model and tech-files

Efficient, concurrent workflow for faster closure

Unified Full-Flow Productivity

Single environment, GUI and netlist for full system design

Full breadth of integrated engines: design, test, analysis, verification

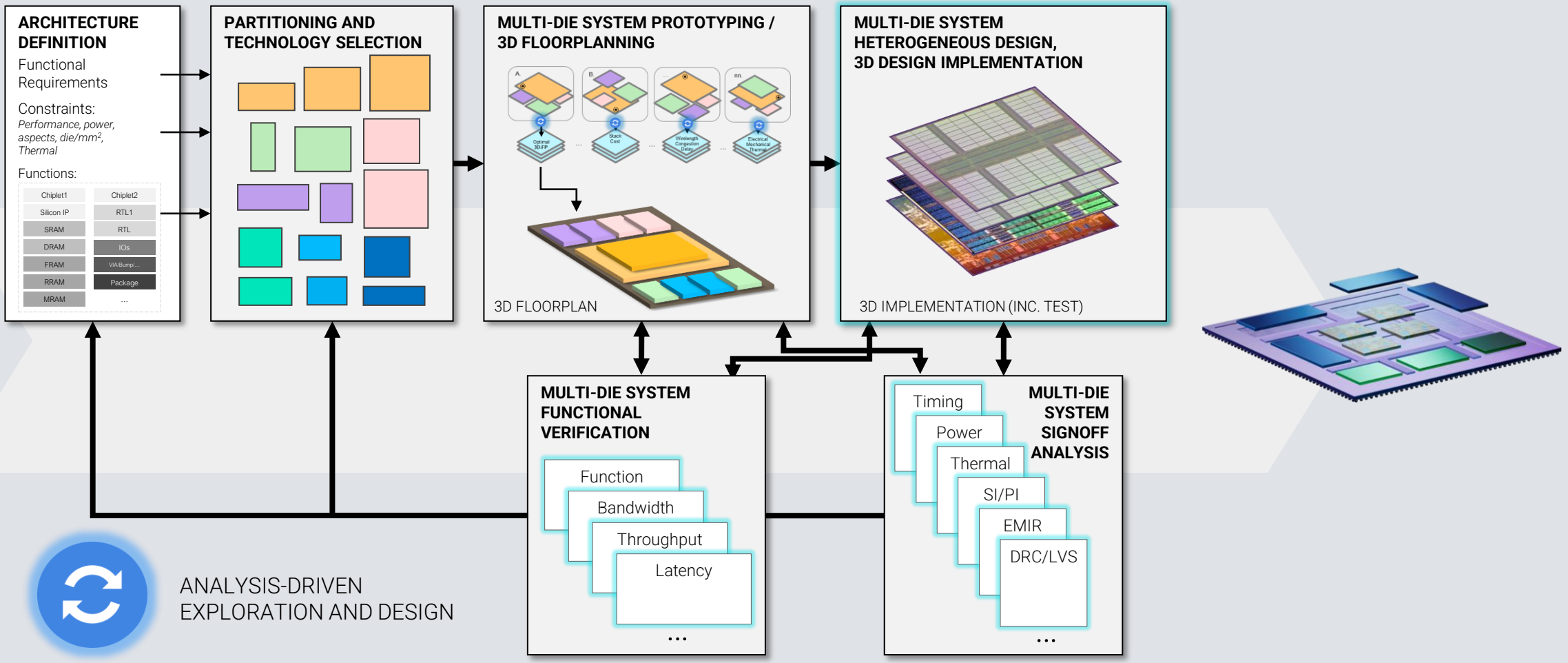
Trusted, Golden-Signoff Analysis

Industry standard technologies – STA, Thermal, EMIR, SI/PI

Fast convergence to optimal PPA/mm3, accelerate tapeout

Enable A Seamless Architecture-to-Design-to-Signoff Journey

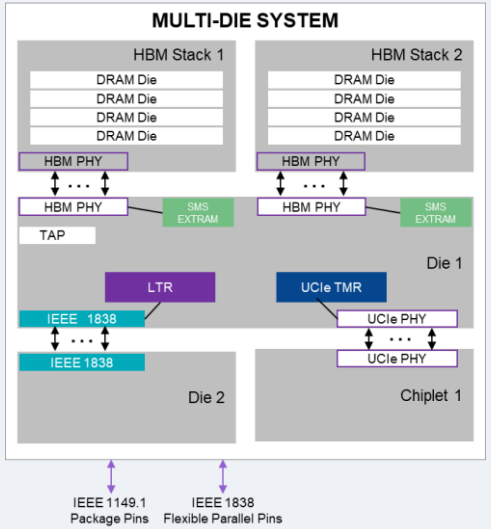
Create, implement, refine, converge



Manufacturing Ramp and Product Reliability

Multi-Die System Test & Repair

Product Quality (KGD, Package, System)



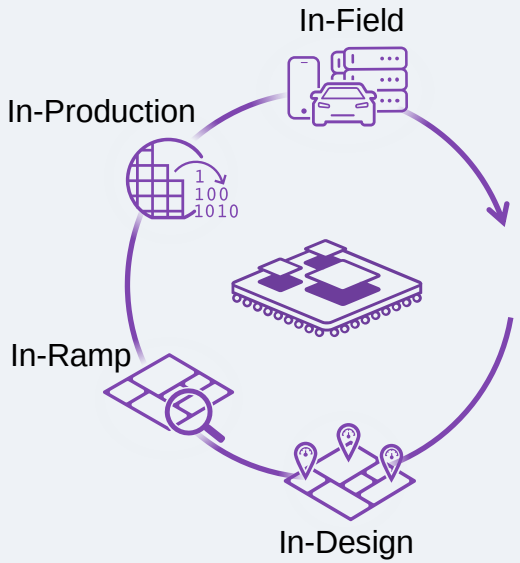
Ensure quality with comprehensive test, debug, repair for multi-die systems

Integrated Test for:
Multiple Dies, Memories, Interconnects, and Full-system

Test Access	Logic-to-Logic	Logic-to-Memory	Via / Bump / Interconnect
IEEE 1838	PHY Monitor, Test & Repair	Ext. Memory BIST & Repair	High volume Lane Test & Repair

Silicon Lifecycle Management

Reliability, Yield, Health

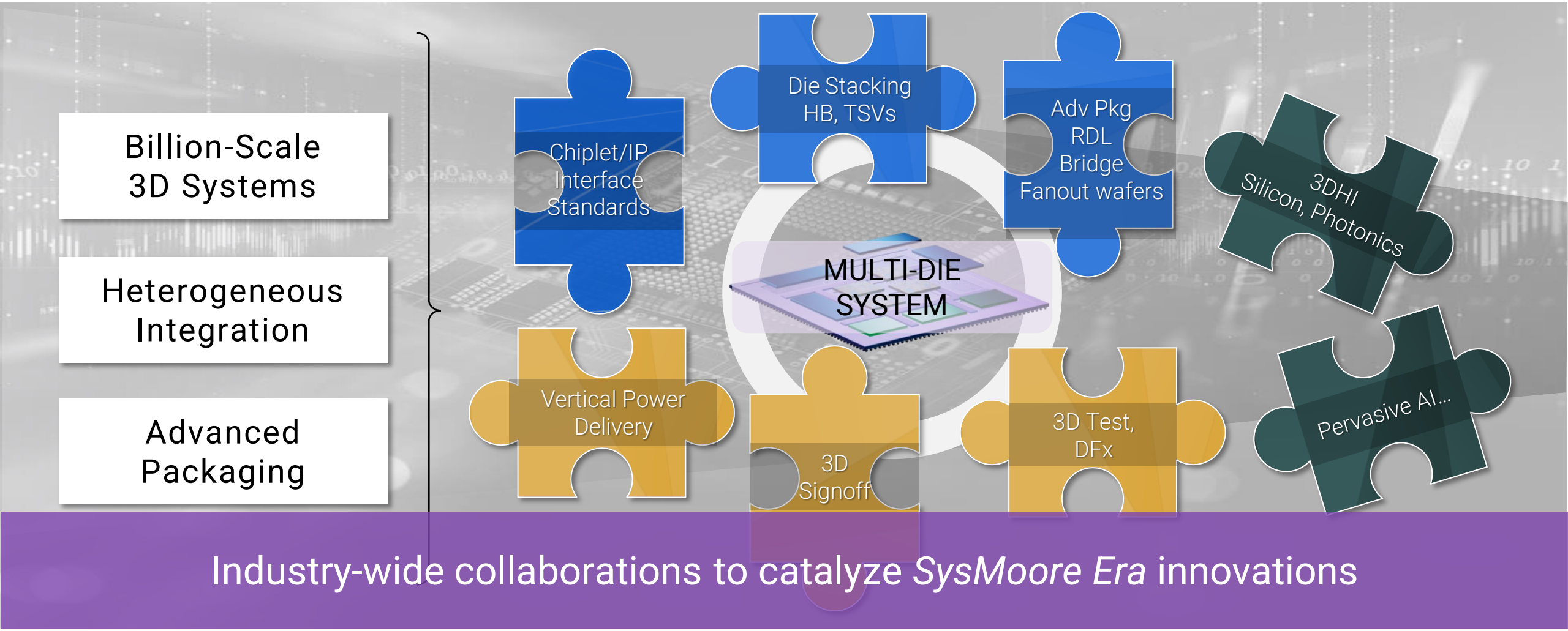


Enhance multi-die system operational metrics through environmental, structural, functional monitoring

Solution Comprises:
Silicon IP, EDA Software, and Analytics Insights

In-Design	In-Ramp	In-Production	In-Field
Power/ Performance Optimization	Yield, Failure Analysis	Volume Test, Quality and Traceability	Optimization, Safety, Security, Maintenance

Summary: Multi-Die Systems – Future of Semiconductors



Thank You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