SIPEARL

Chiplet-based architectures for compute, an ultimate solution for Europe

GSA International Semiconductor Conference

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SiPearl in a nutshell

Building the European energy-efficient HPC microprocessor

Incorporated
In June 2019

Financing
Series-A (to date): €113m

Funded
By the European Union

Key partnerships
Joint-offering with

Arm architecture
Energy-efficiency quick time to market, proven ecosystem

Identified customers
Server manufacturers based on user specifications: First, EuroHPC ecosystem before going global.

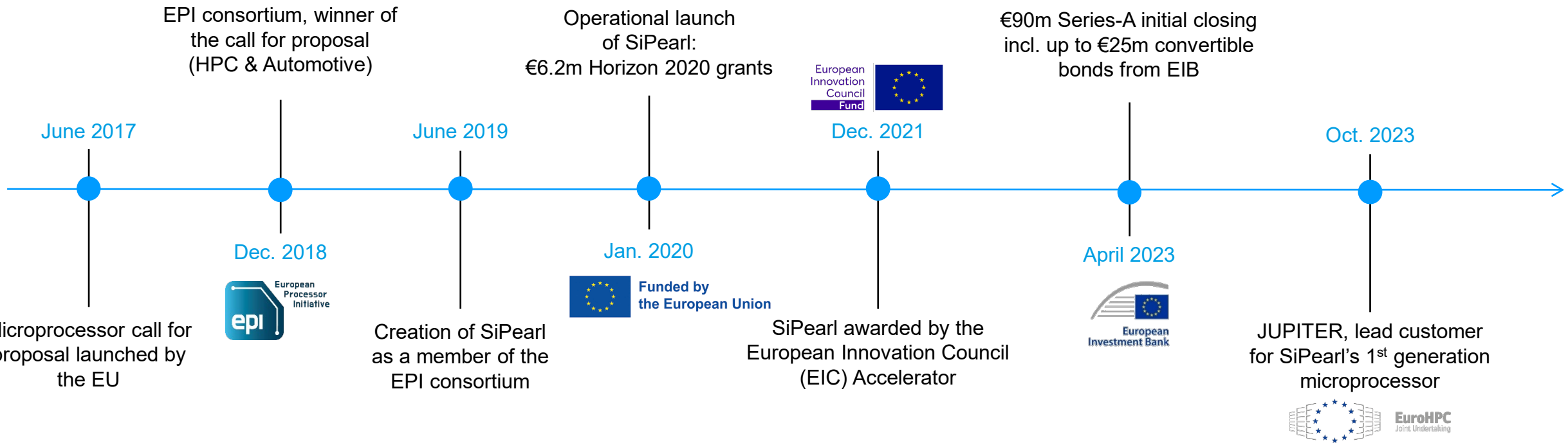
+180
Employees
from

6 locations
Maisons-Laffitte (HQ), Barcelona, Duisburg, Grenoble, Massy, Sophia Antipolis

And soon in Bologna

From a European Union concern to SiPearl launch and growth

Our common goal: fostering the return of high-performance, low-power microprocessor technologies in Europe



Corporate vision and strategy

HPC & AI inference

HPC & AI

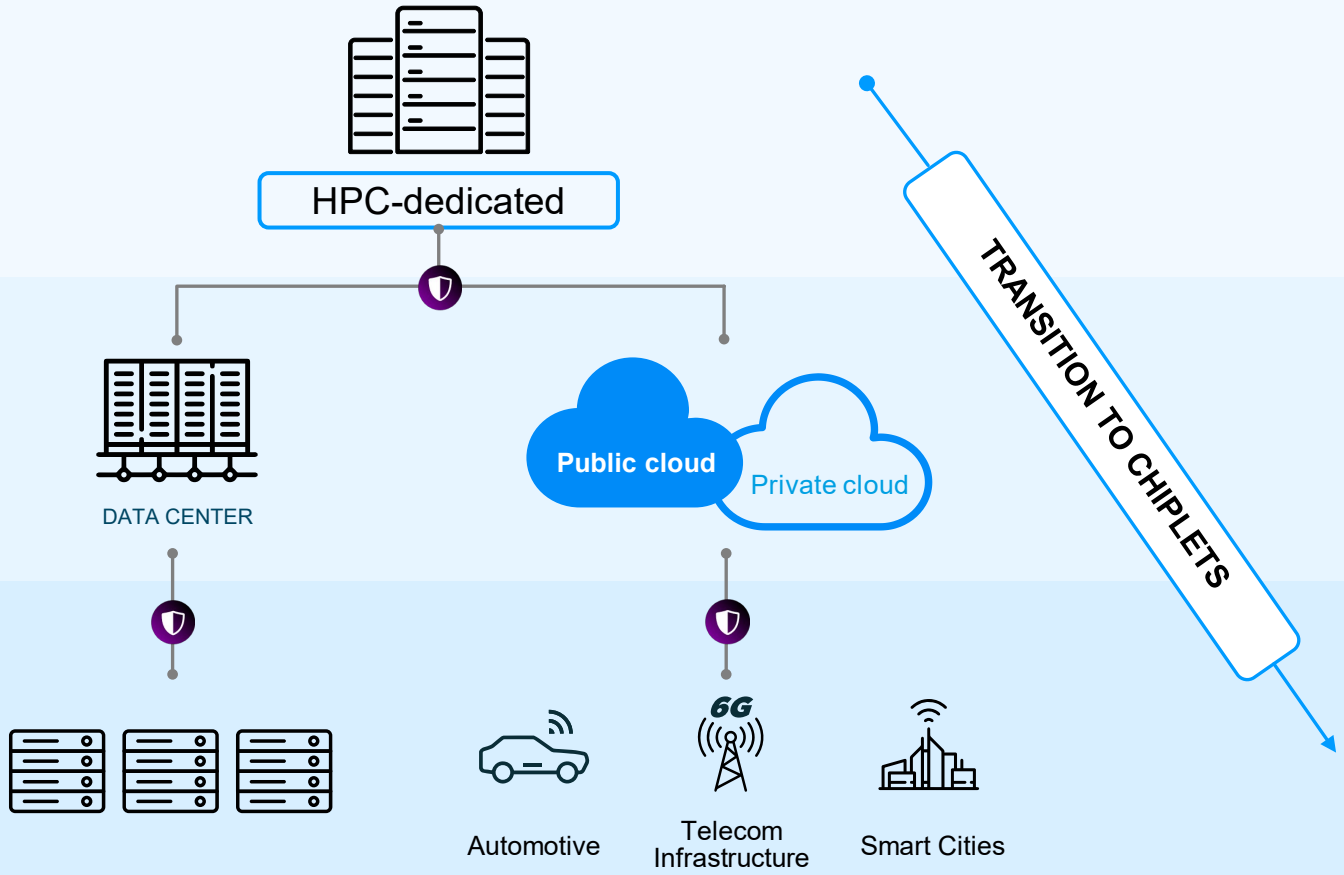
Growth vector: AI Inference in HPC and Data center

Data center-Central

Data centers, private and public cloud

Data center-Edge

Small Compute Farms around 6G infrastructure



Transition to chiplets - benefits

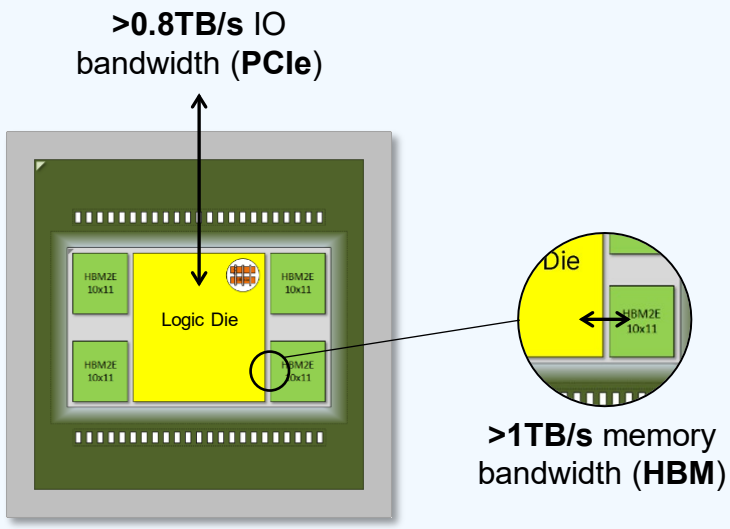
- **Cost:** mixed process nodes, scaling for product line, reuse across product lines
- **Performance:** mix compute and acceleration, better density
- **Power:** best process node per function, scaling of compute and acceleration

Generation 1: architecture vision

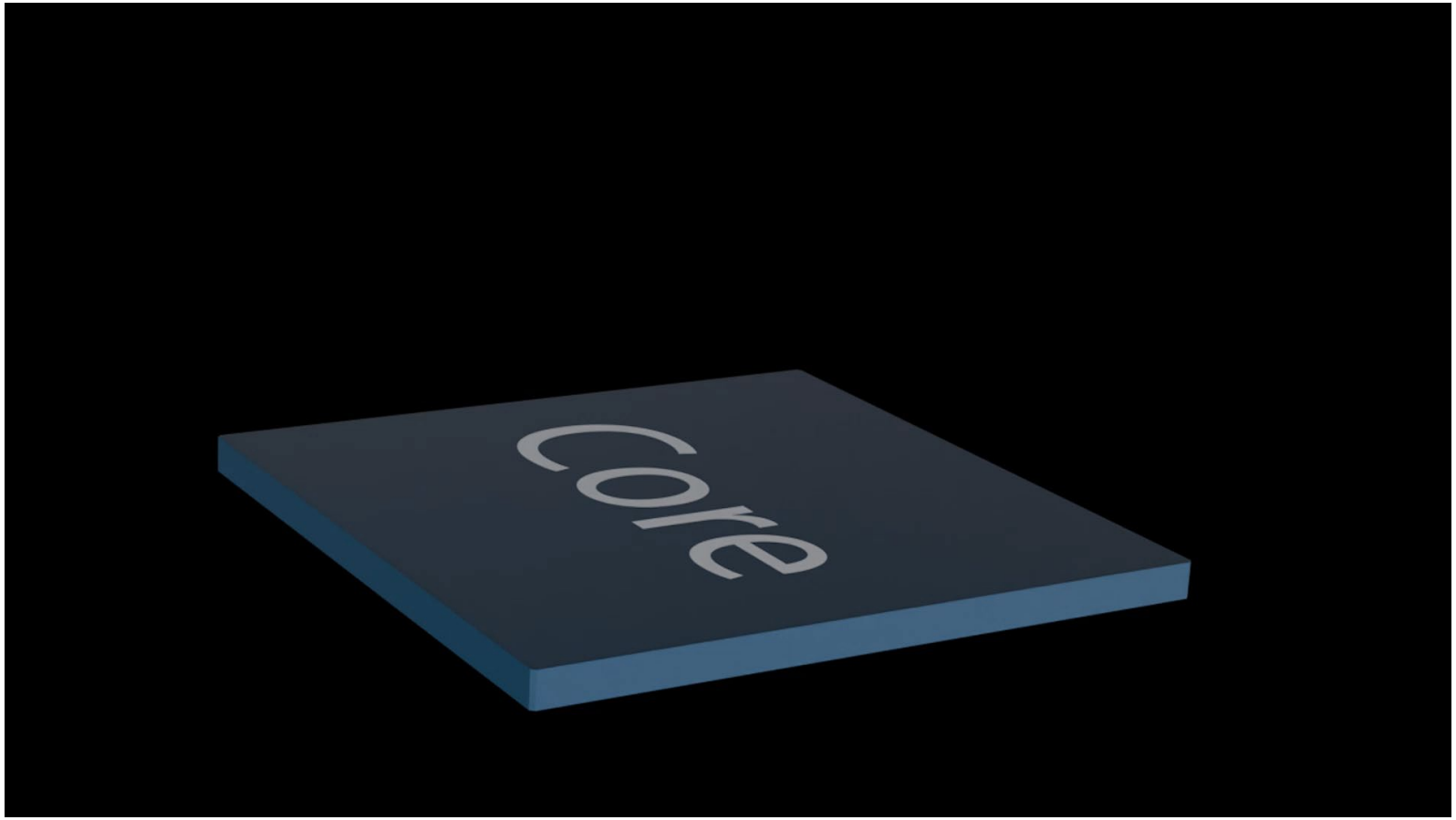
Gen1

HPC & AI

1 logic Die + 4 HBM2E stacks



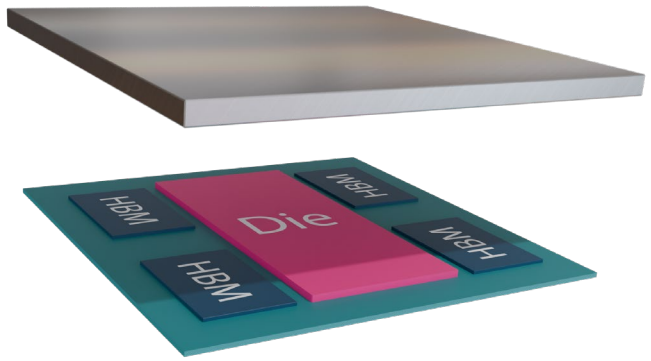
Performance: 3 TFLOPS/**die**



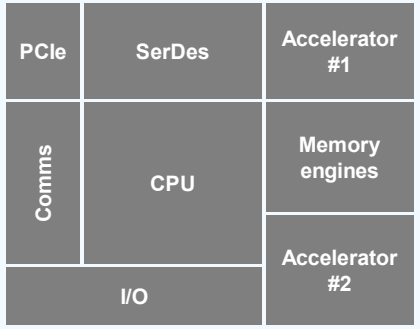
Chiplets change the game for compute

From **monolithic** designs
… to **modular** designs

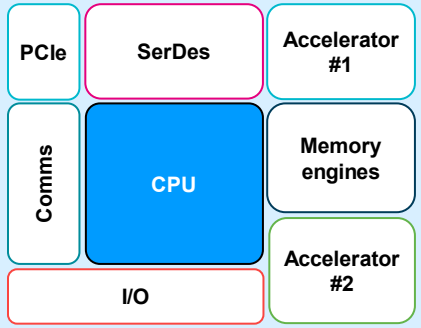
- ✓ Reduced investment costs
- ✓ Lower cost of specialisation
- ✓ Lower production costs
- ✓ Lower supply risks for OEMs
- ✓ Shorter time to market
- ✓ Simpler architectural partitioning



Monolithic chip architecture



Chiplet-based architecture



CHIPLET OPPORTUNITIES FOR VERTICALS

TELECOM & EDGE

- Rethink partitioning with opportunity of heterogenous Radio, Compute and/or AI.
- Antenna in Package
- Increase performance from private 5G to Multi-user MiMo 5G public network

AUTO

- Central Computing and/or Zoning i.e. aggregate functions to reduce number of ECU and vehicle complexity
- Automated Driving - Enabler for ADAS (Advanced Driving Assistance Systems)
- Aggregation of functions e.g. connectivity

AERO & DEFENSE

- Possibility to mix military & commercial
- Easier demarking for end product when targeting sovereign or export product
- Cyber : A chiplet can be the Root of Trust of the SoC allowing to use commercial source Chiplets for noncritical assets

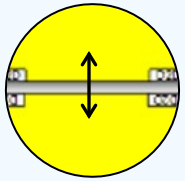
Next generations: architecture vision

HPC/AI inference & Data centre

Chiplet designs increase the number of transistors per package (>6X)

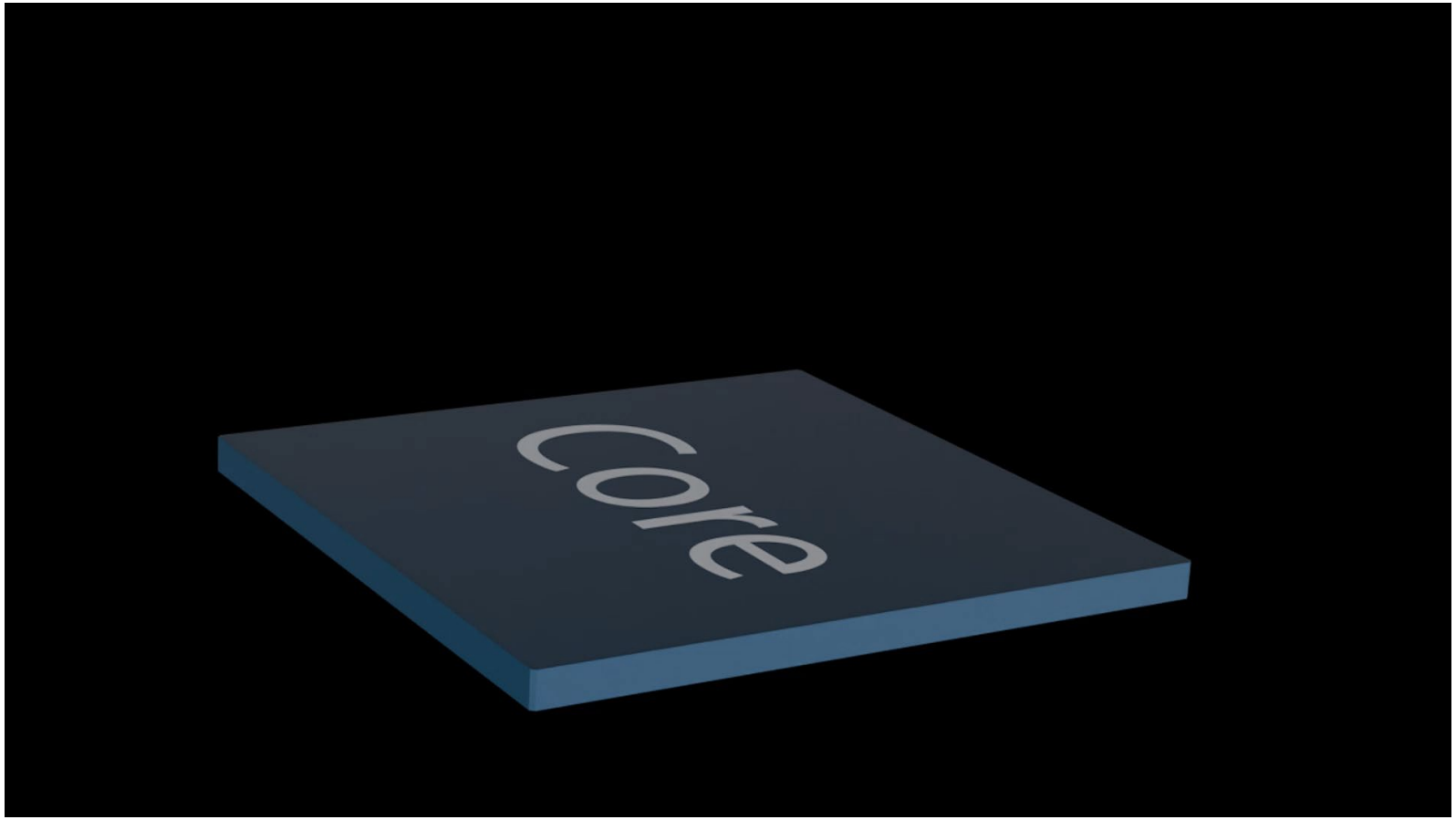
HBM memory bandwidth: 16x DDR

UCIe to standardize chiplet interfaces



PCIe/CXL double generation over generation to maximize injection bandwidth

NoC design >2X generation over generation to realize injection and memory bandwidth

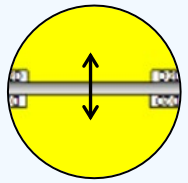


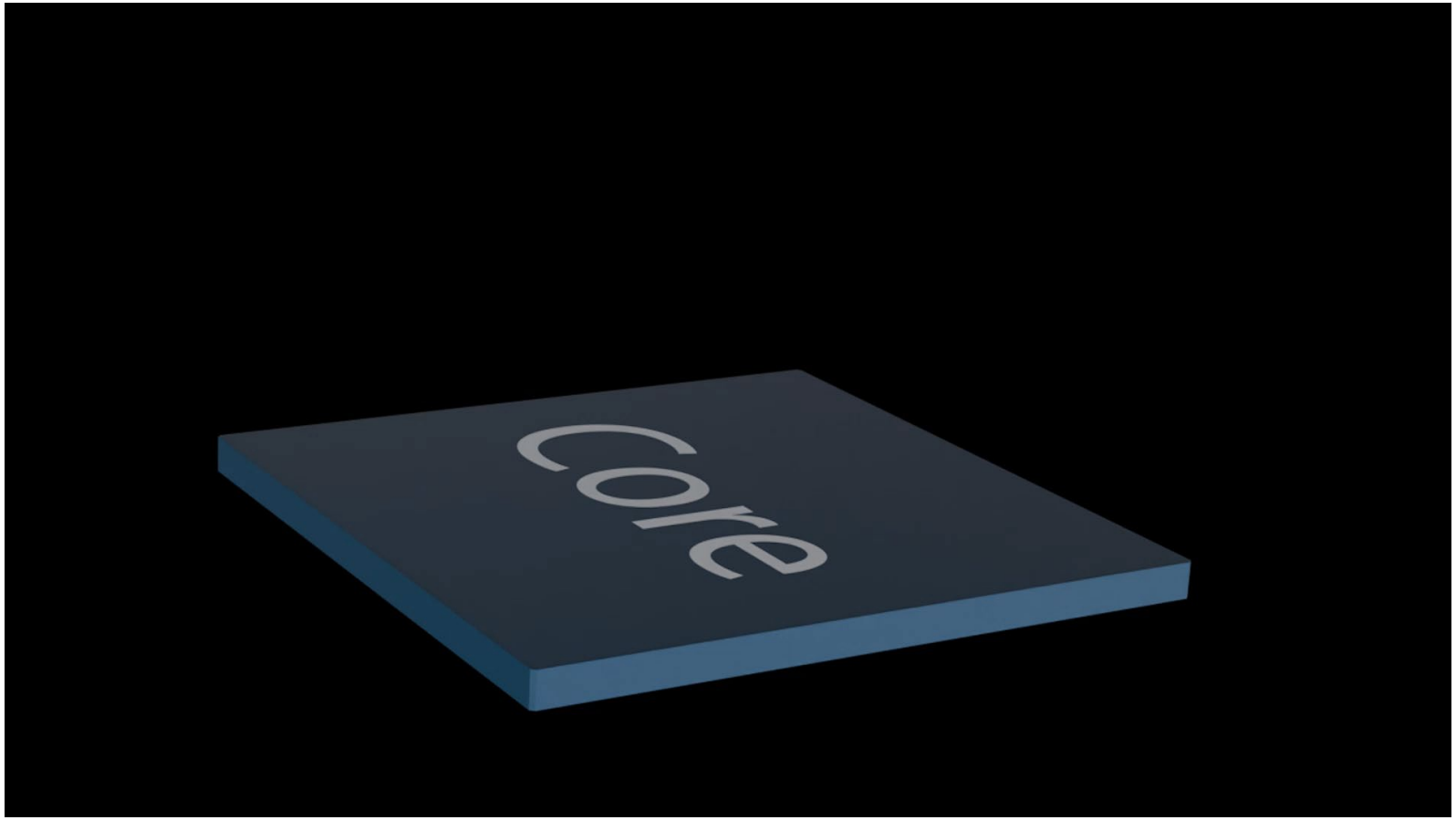
Next generations: architecture vision

Automotive & Telecoms

Chiplet designs to optimize compute and performance / watt:

- Reuse compute across product lines – lower cost and faster time to market
- Scalability up and down product line, both compute and acceleration
- Compute and interconnect designed in the appropriate process nodes, with staggered update
- UCIe to standardize chiplet interfaces





Platform evolution to Automotive & Telecom

CPU Gen1
(2024)

CPU Gen2
(2025)

CPU Gen2
(2025)

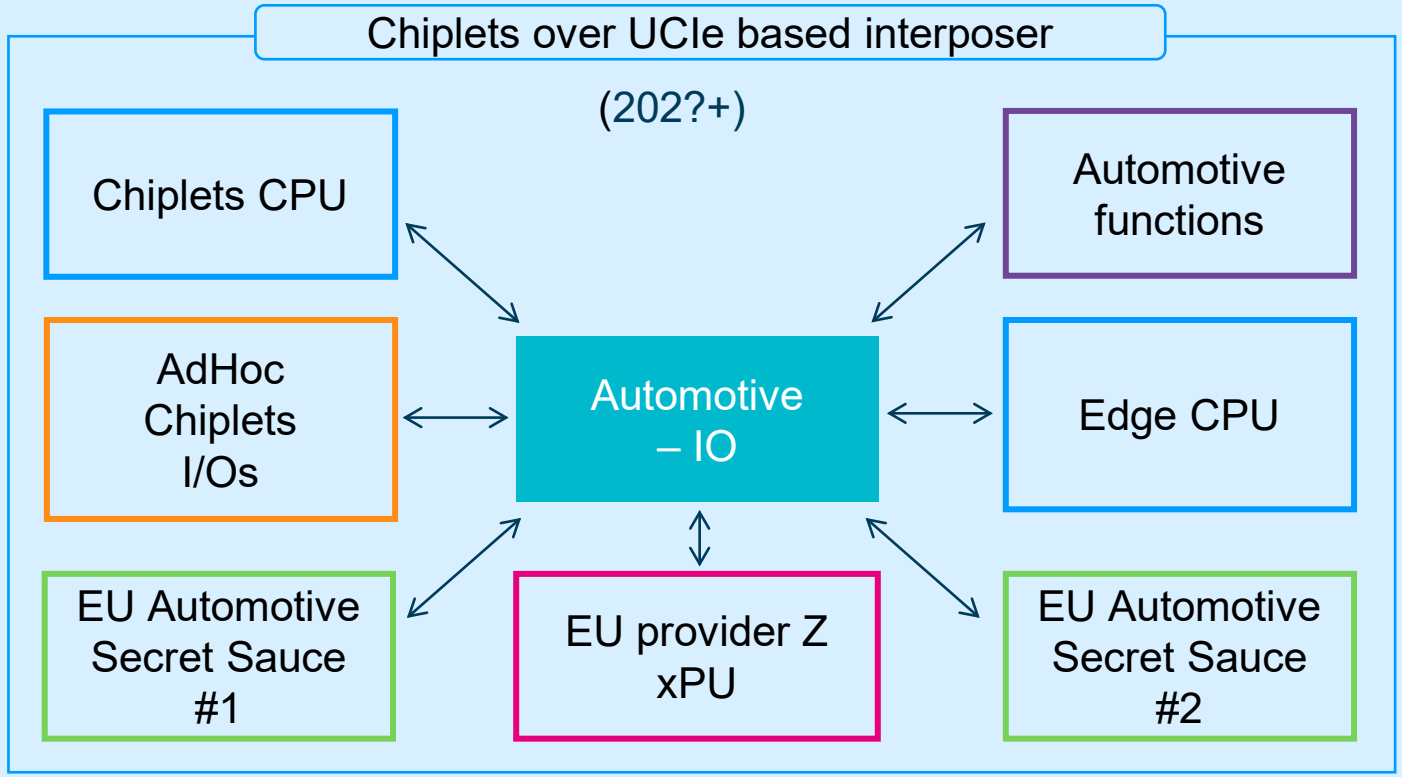
GPU
(2025)
US provider

Module / Board

Exascale (2025+)

EPI1

EPI2



Automotive-Compute platform (202?+)

EU program Next Phases

About… SiPearl

SiPearl is building the world first energy-efficient HPC-dedicated microprocessor designed to work with any third-party accelerator (GPU, artificial intelligence, quantum). This new generation of microprocessors will first target EuroHPC Joint Undertaking ecosystem, which is deploying world-class supercomputing infrastructures in Europe for solving major challenges in medical research, generative AI, security, energy management and climate while reducing its environmental footprint.

SiPearl is working in close collaboration with its 30 partners from the European Processor Initiative (EPI) consortium - leading names from the scientific community, supercomputing centres and industry - which are its stakeholders, future clients and end-users.

SiPearl employs more than 180 people in France (Maisons-Laffitte, Grenoble, Massy, Sophia Antipolis), Germany (Duisburg) and Spain (Barcelona).

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