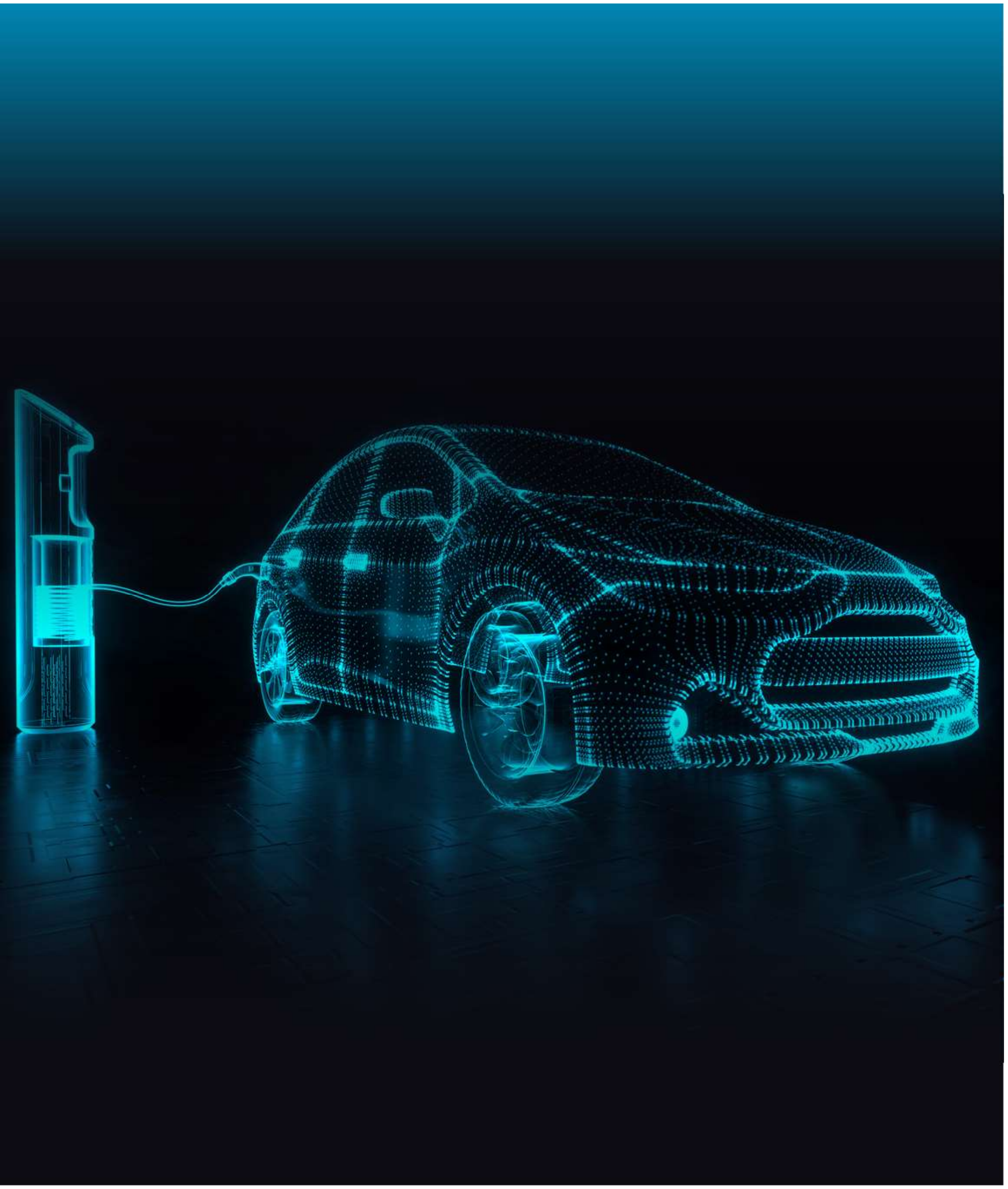


High Reliability Materials for Automotive Semiconductors

Oreste Donzella

Executive Vice President, EPC Group

KLA Corporation

GSA International Semiconductor Conference

March 2024

KLA at a Glance

Founded in
1976

Headquarters in
Milpitas, CA

18
Regions

~15,000
Employees

$9.6B
CY23 Revenue

>65%
PhD/Master’s among professional roles

Forbes 2022
WORLD’S BEST EMPLOYERS
POWERED BY STATISTA

TIME
WORLD’S BEST COMPANIES
IN PARTNERSHIP WITH statista 2023

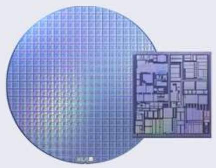
FORTUNE
WORLD’S MOST ADMIRED COMPANIES™
2023

FORTUNE 500
2023

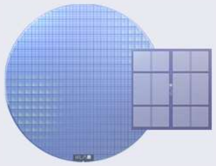
Forbes 2022
WORLD’S TOP FEMALE FRIENDLY COMPANIES
POWERED BY STATISTA

KLA’s Role in the Electronics Ecosystem

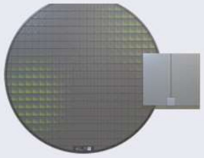
CHIPS



Logic | Foundry

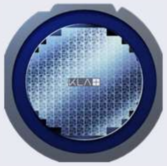


Memory

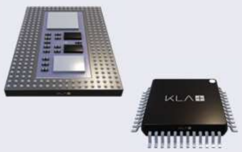


Specialty | Legacy

WAFER-LEVEL PACKAGING

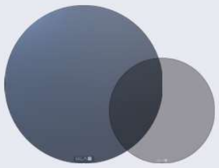


COMPONENTS



PRINTED CIRCUIT BOARDS

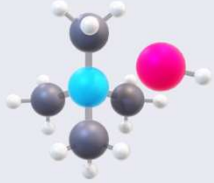
WAFERS



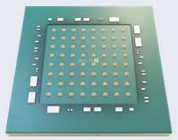
RETICLES

SEMI OEMs

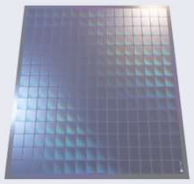
CHEMICALS | MATERIALS



IC SUBSTRATES



FLAT PANEL DISPLAYS



END MARKETS

- Data Center
- Artificial Intelligence
- 5G Infrastructure
- Mobile
- Automotive
- PC / Tablet
- Metaverse (AR/VR)

New KLA UK Manufacturing and R&D Center in Newport, UK

>$100 million USD investment

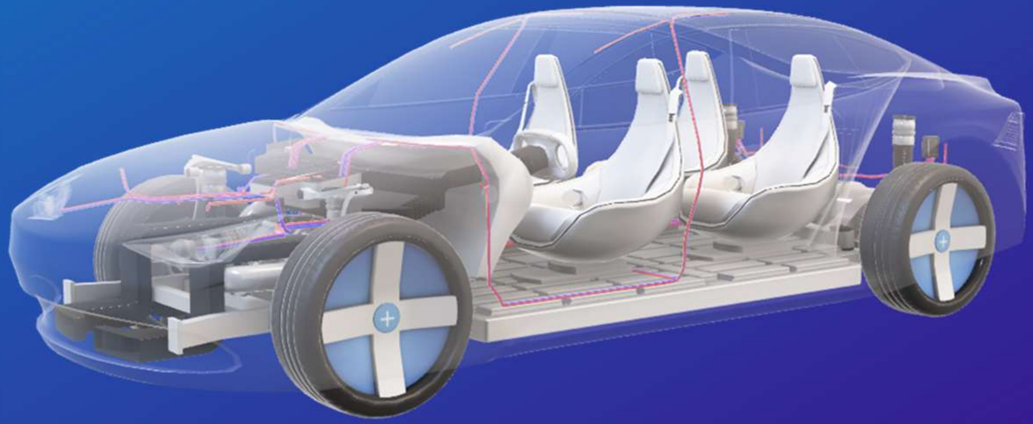
Completion early 2025

67,000 sq ft cleanroom

Up to 750 employees

Support growth of the SPTS organization, focused on specialty semiconductors and wafer level packaging

KLA in Automotive



Automotive Innovation is Dependent on Semiconductors

Safety and Security

- Zero in-process defects
- Zero market failures

Electrification: Zero Emissions

- More miles on battery
- SiC/GaN power semi devices

Autonomous Drive and ADAS

- Leading-edge CPU/GPU, more sensors
- In-car networking

Networking: Connected Car

- 5G capable
- Big data processing in the cloud

>100
connected electronics control units (ECU)

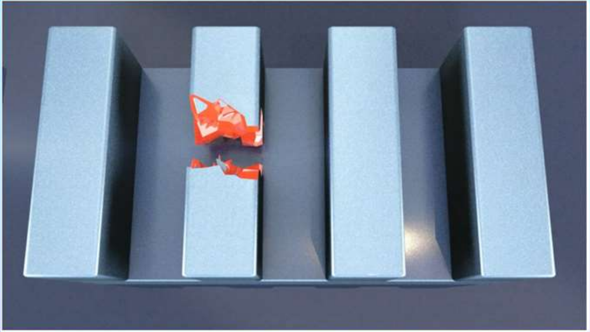
6,000-10,000
semiconductors per vehicle

Qualification
2 years vs 5+ years

Innovations
>80% enabled by semiconductors

Potential Reliability Defects Must Be Found to Meet Quality Goals

Test Escapes



- Hard killer defects in a test coverage gap
- Function of yield and test coverage

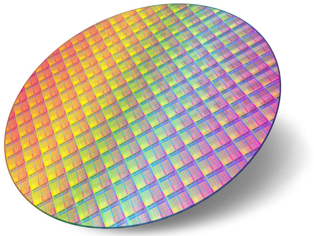
Latent Reliability Defects

- Become activated some time after test
- Usually requires statistical approach

Multi-level Collaborations to Advance Automotive Roadmap

Car Makers

Chip Companies



IDMs

Foundries

Fabless

KLA

Tier 1 Suppliers

800V SiC traction inverter, courtesy Vitesco

Other 3rd Parties

Test companies

MICHIGAN

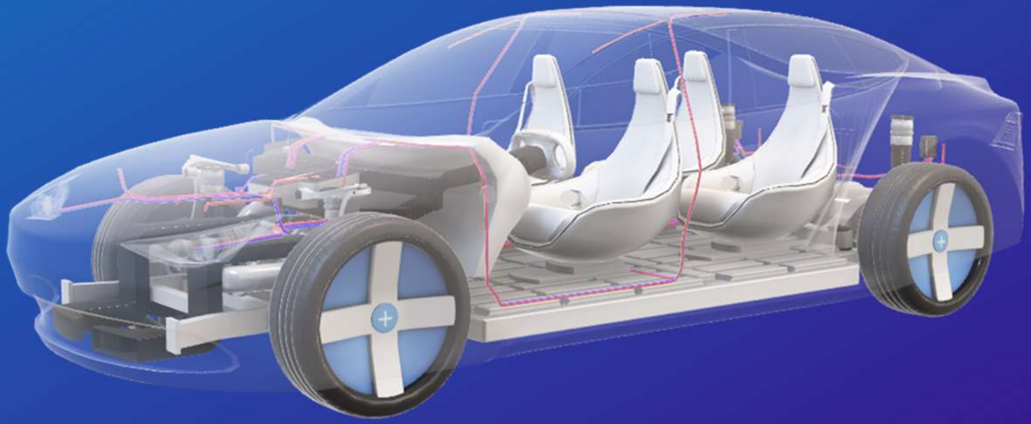
imec

semi

Automotive Electronics Council
Component Technical Committee

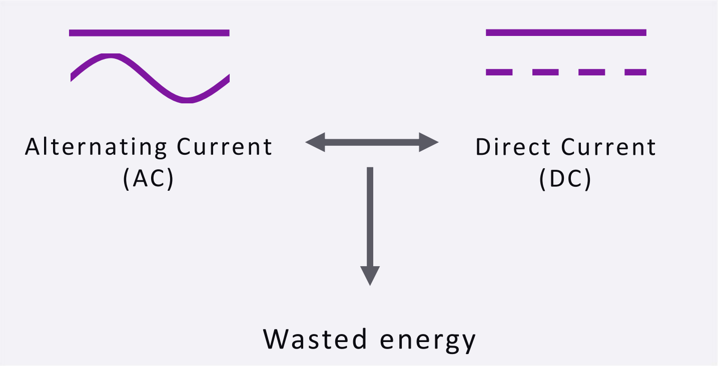
Entire supply chain for automotive required to solve difficult problems

Transition to SiC



Power Conversion is Everywhere

Power conversion changes electricity from the form available to the form required for a product to perform



Alternating Current (AC)

Direct Current (DC)

Wasted energy

Minimizing wasted watts can result in significant energy savings[1]

The Wide-Bandgap (WBG) Efficiency Advantage

- Data centers
- Industrial electric motors
- Automobiles
- AC power adapters

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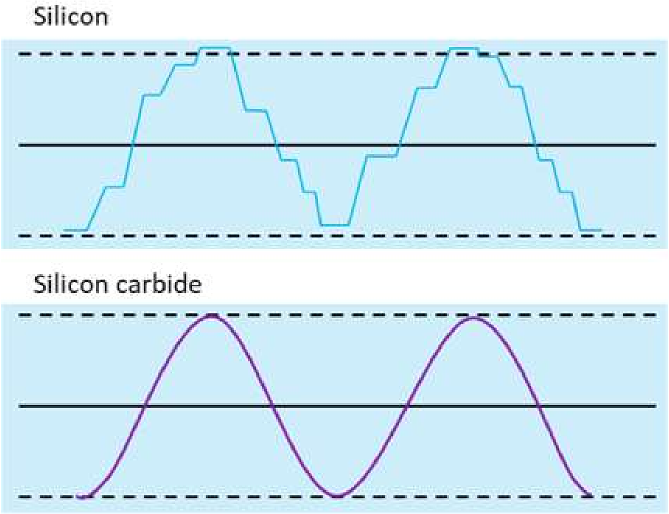
[1] https://spectrum.ieee.org/silicon-carbide

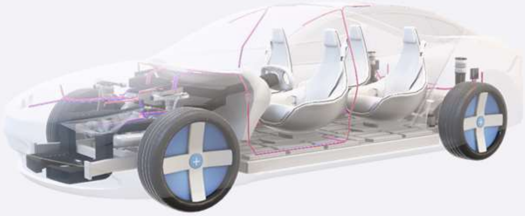
Why Silicon Carbide is the new Automotive Power Material?

WBG allows faster switching



EV System Benefits

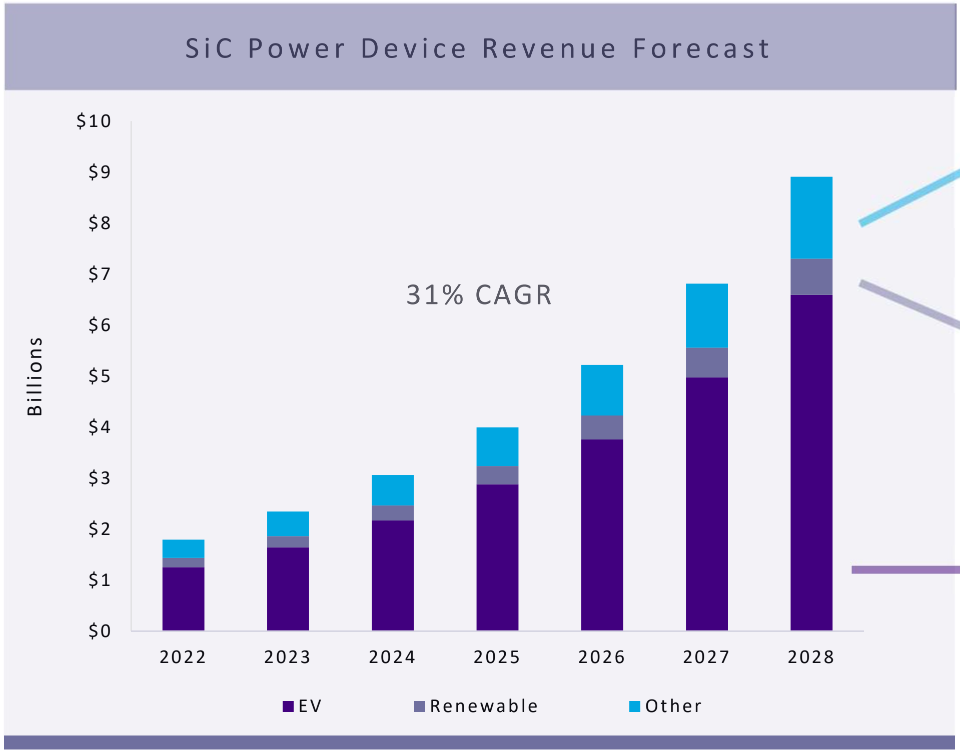
- 6-12% smaller battery (same range)
- Smaller inverter, cooling system
- 6-12% better MPGe



References:
1. Rohm white paper, "Application benefits of using 4th Generation SiC MOSFET's"
2. EE006920 "88 Kilowatt Automotive Inverter with New 900 Volt Silicon Carbide MOSFET Technology"

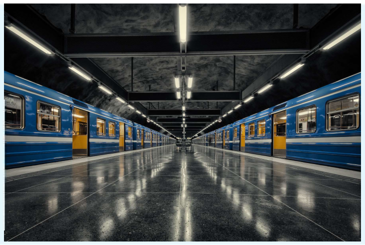
Faster switching improves efficiency and provides better thermal performance

Silicon Carbide (SiC) Brings Incredible Opportunity



SiC Power Device Revenue Forecast

Source: Yole 2023



- Rail
- Motor control
- Data center
- Smart grid

Renewables

- Inverters for wind
- Inverters for solar

Electric vehicles (EV)

- Traction inverter
- Onboard charger
- DC/DC converter

Higher Efficiency | 2-4x smaller system form factor | Less heat generation

But SiC Has a Yield Problem

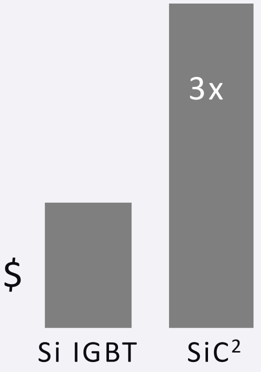
Typical Yield by Step[1]

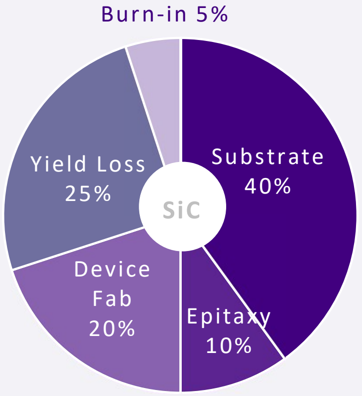
Epitaxy	85%
Device fab: wafer (scrap)	80%
Device fab: probe	82%
Dicing	93%
Packaging	98%
Final test / burn-in	97%

Overall Yield <50%

Low Yield Brings Challenges

Cost





Reliability

Escapes = f (yield, test effectiveness)[3]

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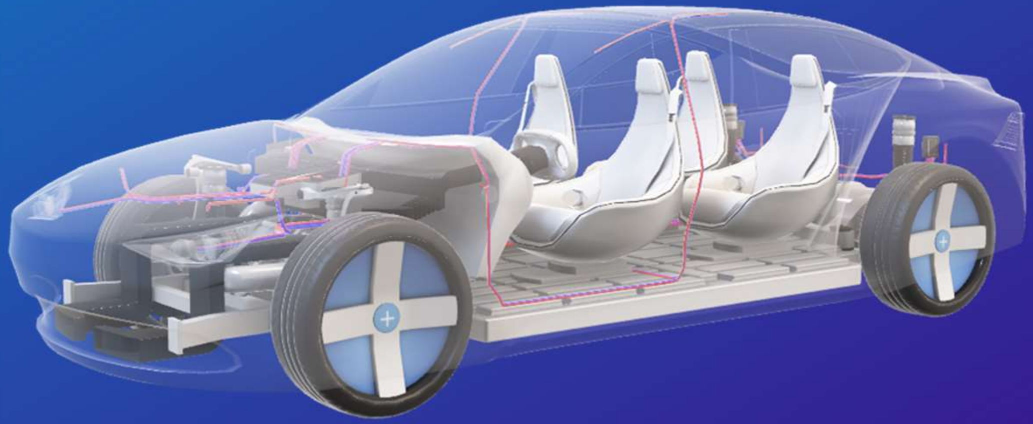
[1] SiC yield and cost are typical values (2023), compiled from Yole, JP Morgan, PGC Consultants, KLA data, and other sources. Large variation from fab-to-fab.

[2] At equivalent performance for EV traction inverter mission profile compared to comparable Si IGBT device.

[3] See, for example, Williams-Brown or Seth-Agrawal test escape models

Yield impacts both cost and reliability

KLA SiC Solutions



Optimized Process and Process Control Drive Yield Improvement

- Substrate and epitaxy
- Device fab
- Dicing
- Packaging
- Final test / burn-in

Highlights from KLA's SiC Portfolio

Process


plasma etch


plasma dicing


PECVD


PVD

Inspection

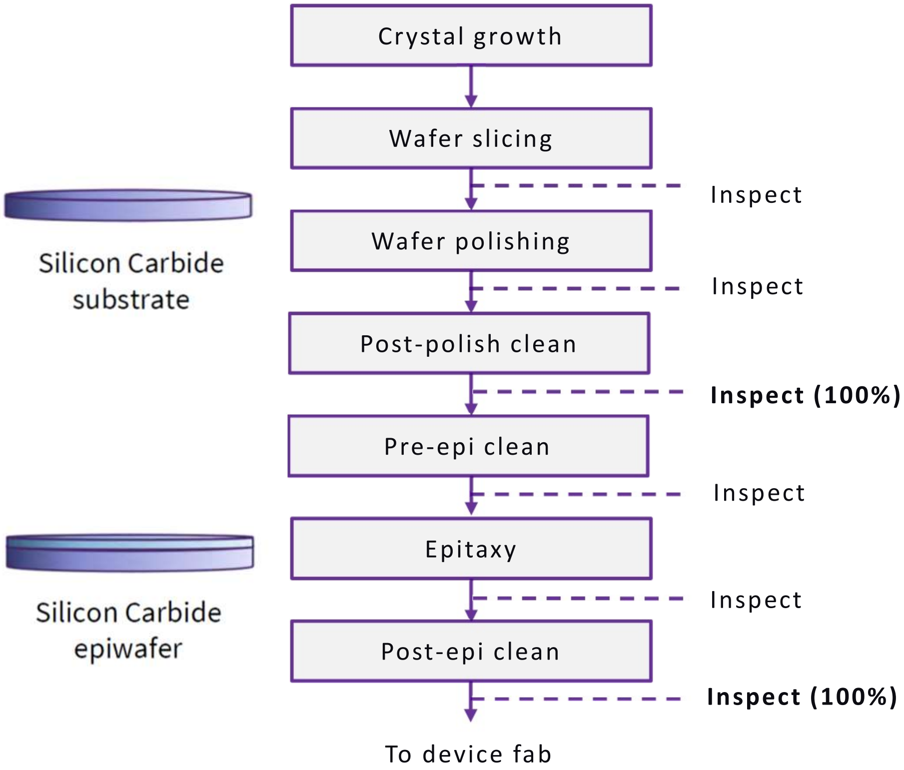
inspection solutions for substrate/epitaxy, patterned wafer and inline defect screening

Metrology


metrology solutions for wafer shape, films, overlay, CD, implant and analytics

Yield Improvement Starts with High Quality Substrates

- **Substrate and epitaxy**
- Device fab
- Dicing
- Packaging
- Final test / burn-in



Crystal growth

Wafer slicing

Inspect

Wafer polishing

Inspect

Post-polish clean

Inspect (100%)

Pre-epi clean

Inspect

Epitaxy

Inspect

Post-epi clean

Inspect (100%)

To device fab

Silicon Carbide substrate

Silicon Carbide epiwafer

>50% of total yield loss is from substrate and epitaxy defects

- Surface defectivity
- Crystal defectivity
- Surface roughness, haze
- Wafer shape, stress
- Epi defectivity
- Epi thickness
- Epi uniformity

Complicated (and expensive) SiC substrate and epitaxy require 100% inspection

Defect Inspection Focused on Substrate and Epitaxy Quality

Defect Inspection Strategy

Substrate Quality

Buffer Quality

Epitaxy Process

Reactor Cleanliness

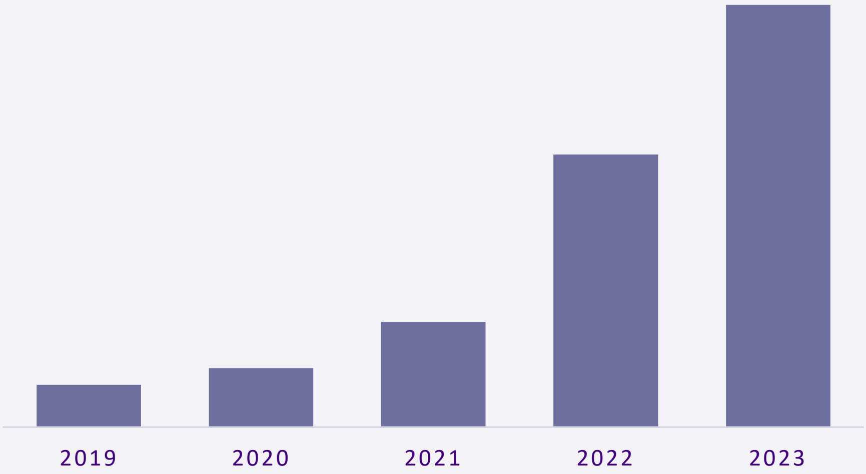
Surface Defectivity

- Scratches
- Particles
- Surface roughness (haze)

Crystalline Defectivity

- Micropipes
- Dislocations
- Stacking faults
- Others

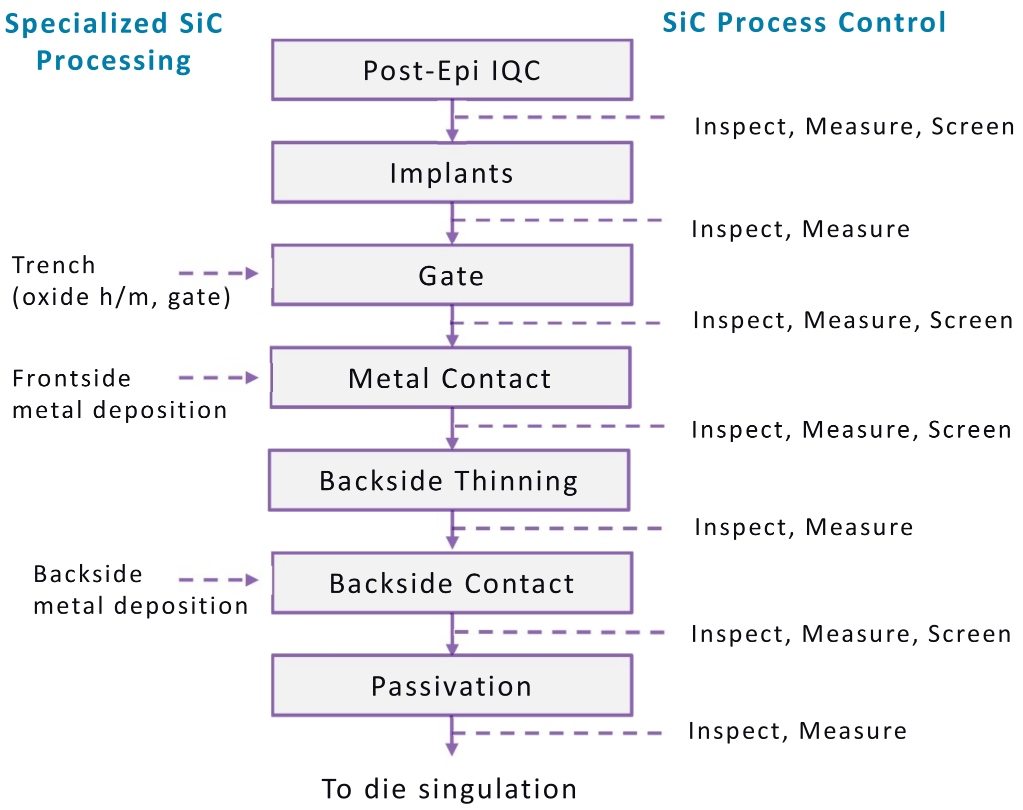
KLA Substrate/Epitaxy Defect Inspection Tools for Power SiC (units, cumulative)



Candela systems are being adopted for both substrate and epitaxy yield improvement

SiC Device Fab

- Substrate and epitaxy
- Device fab
- Dicing
- Packaging
- Final test / burn-in



Specialized SiC Processing

SiC Process Control

Post-Epi IQC

Inspect, Measure, Screen

Implants

Inspect, Measure

Trench (oxide h/m, gate) → Gate

Inspect, Measure, Screen

Frontside metal deposition → Metal Contact

Inspect, Measure, Screen

Backside Thinning

Inspect, Measure

Backside metal deposition → Backside Contact

Inspect, Measure, Screen

Passivation

Inspect, Measure

To die singulation

Required Process Control

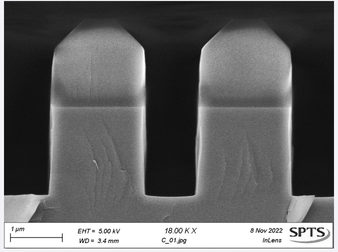
- Product wafer inspection
- Monitor wafer inspection
- Wafer shape/stress metrology
- Overlay metrology
- Shape (CD, SWA) metrology
- Films metrology
- Implant metrology

Specialized process and process control required for improving device yield during manufacturing

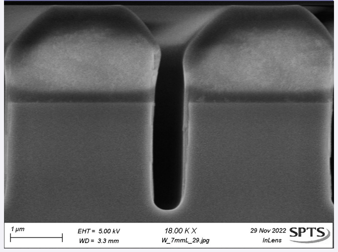
Specialized SiC Processing: Trench Etch

Tailored Profile and No Micro-Trenching

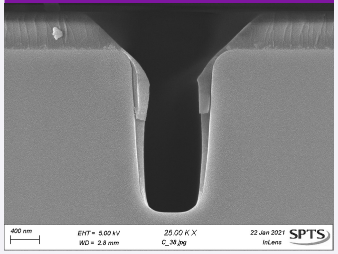
Flat Base



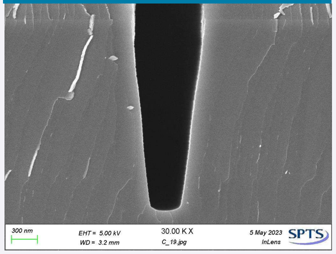
Rounded Base



Rounded Base & Top

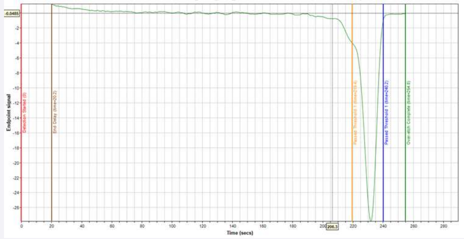


Tapered Etch

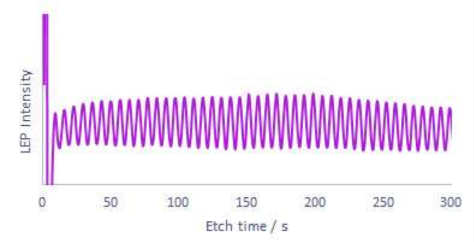


Endpoint Control – Repeatable in Production

Hard Mask Open - OES Endpoint (1st Derivative)



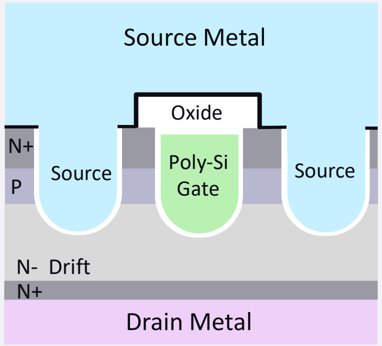
Laser Endpoint – Trench Depth Monitoring



Patent-protected hardware and novel chemistries for productivity and improved device performance

Specialized SiC Processing: Frontside Metal Film Deposition (PVD)

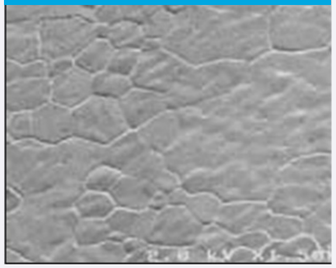
Frontside Metal Applications



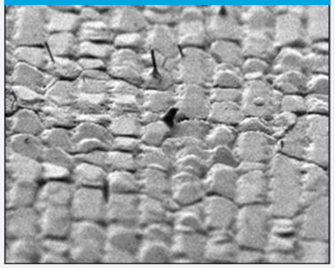
- Ni or NiV: silicide contact
- Ti/TiN: barrier
- Thick Al (3-5 µm): gate/source contact

Spotlight on Thick Aluminum for Gate

SPTS Sigma®, 4 µm Al

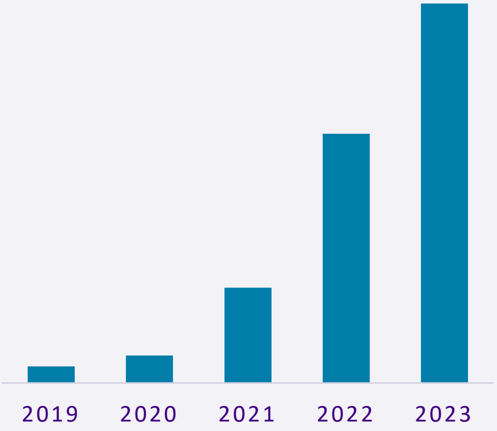


Competitor, 4 µm Al



- Stress relief by grain growth only
- Low whisker levels for improved yield
- Deposition rate >1.4 µm/min, no cool steps
- Single chamber process

Frontside Metal PVD for Power SiC (units, cumulative)



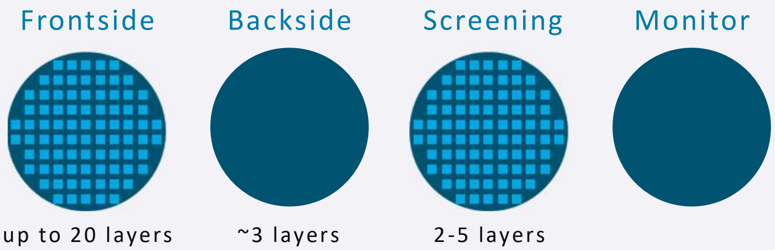
Low whisker film at high throughput provides 30% COO reduction for thick aluminum

SiC Patterned Wafer Inspection for Yield Improvement and Screening

Defect Inspection Strategy

Key defects of interest:

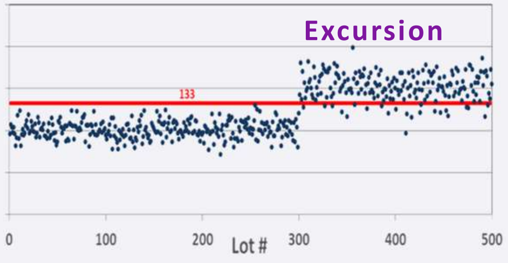
- Result in leakage channels in the z-direction
- Substrate and epitaxy defects transferred to device fab
- Gate oxide defects impacting both yield and reliability

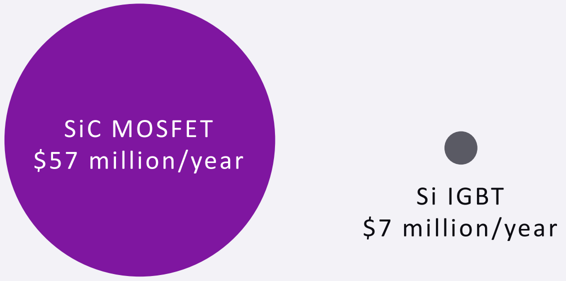


Expensive Starting Wafer Means Excursions Get Expensive Quickly

Annual cost of scrapped wafers assuming:

- 15K WSPM
- 92% line yield
- 80% probe yield





SiC MOSFET
$57 million/year

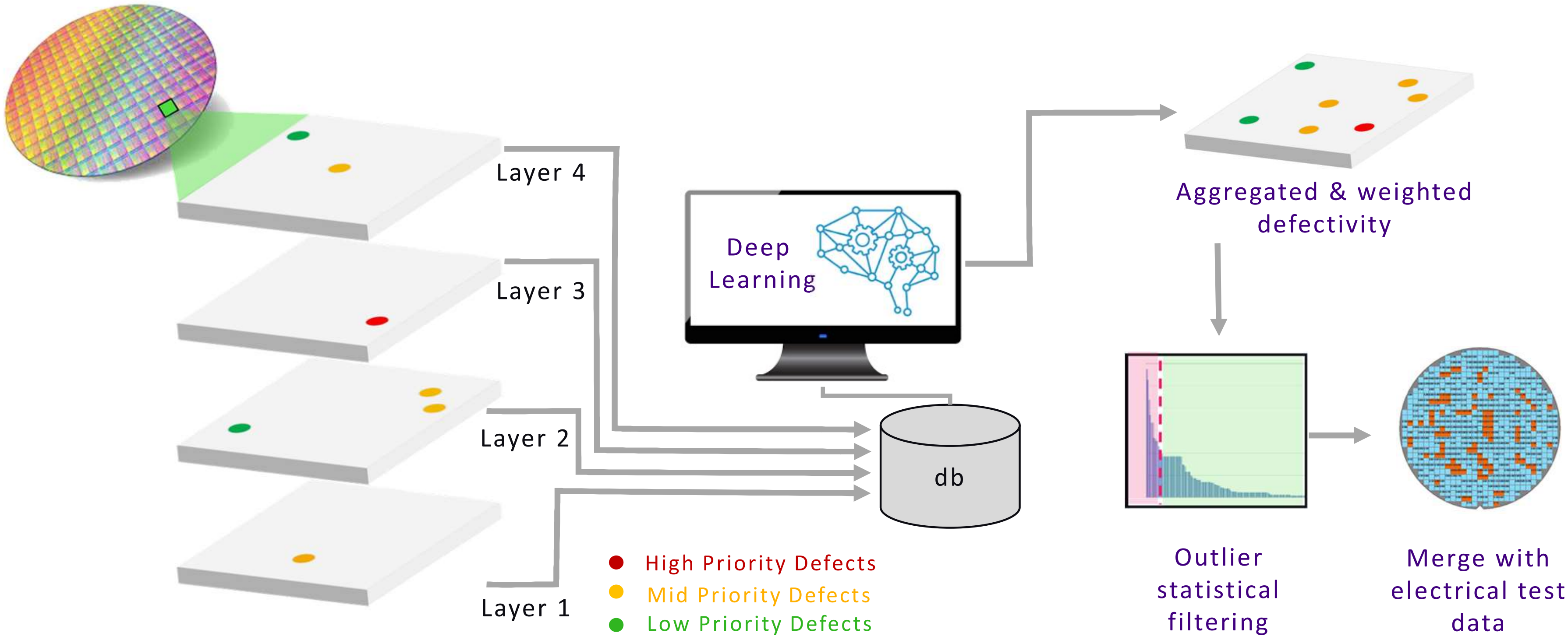
Si IGBT
$7 million/year

Assumptions:

- IC Knowledge Fab Cost Model, KLA excursion model
- SYSTEMPlus consulting, report SP19449
- Cost- based model: does not include lost revenue

Advanced defect inspection required for reducing excursions, yield improvement and screening

I-PAT® Inline Defect Screening Proven for Automotive



Layer 4

Layer 3

Layer 2

Layer 1

Deep Learning

db

● High Priority Defects
● Mid Priority Defects
● Low Priority Defects

Aggregated & weighted defectivity

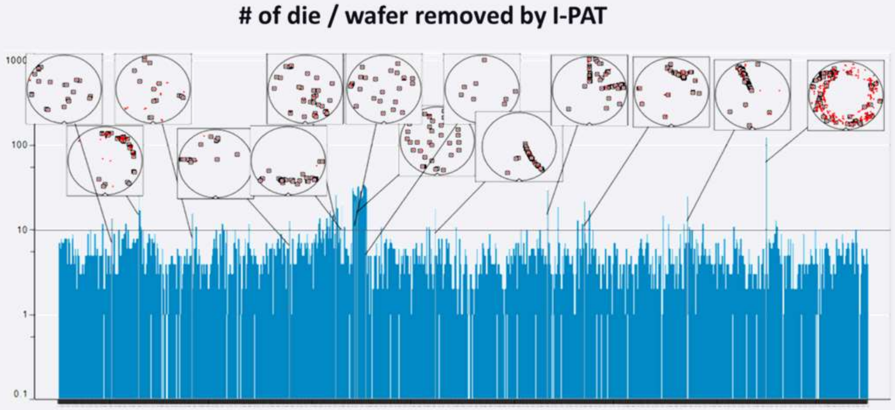
Outlier statistical filtering

Merge with electrical test data

Each die is scored based on aggregate defectivity

Adoption of I-PAT Methodology for SiC Quality Control

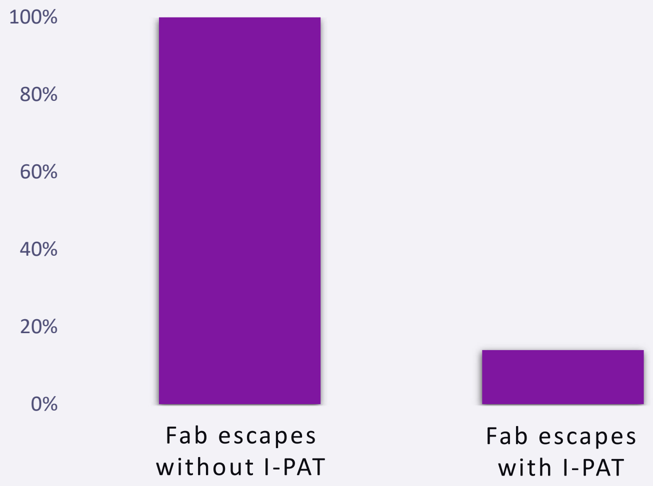
I-PAT provides a safety net to reduce escapes (MCU example)



Physical wafer ID (1400 wafers)

International Test Conference
September 25-30, 2022
Hybrid/Disneyland, Anaheim, CA

86% reduction in potential escapes* (SiC example)

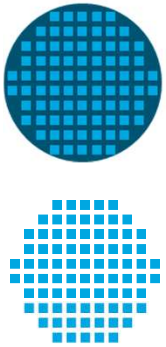


*Results from SiC proof-of-concept investigation

I-PAT screening removes at-risk die to reduce escapes

Die Singulation, Packaging and Test

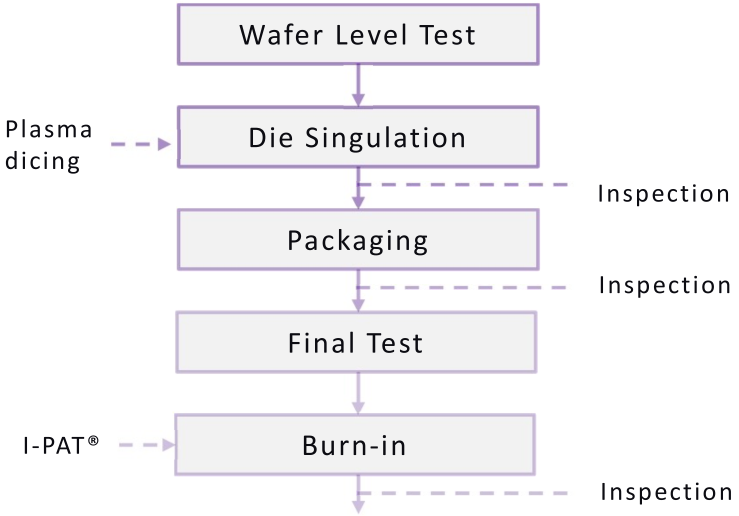
- Substrate and epitaxy
- Device fab
- Dicing
- Packaging
- Final test / burn-in



Multichip module

Image: Borg-Warner

Discrete module



Wafer Level Test

Plasma dicing → Die Singulation

Inspection

Packaging

Inspection

Final Test

I-PAT® → Burn-in

Inspection

Optimizing Known Good Die

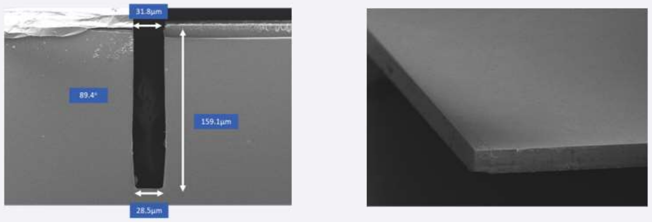
- Plasma dicing avoids chips and cracks from mechanical dicing
- Die edge inspection
- Packaging inspection
- Screening to optimize burn-in and final sort

Only "Known Good Die" should move to next steps in assembly

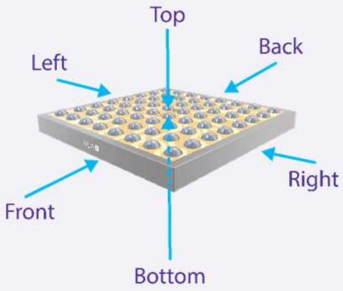
SiC Die Singulation Challenges Bring Opportunities for Innovation

Plasma Dicing for Stronger, Cleaner Die

Quality	▪ No mechanical damage ▪ Fewer particles
Smaller kerf width	▪ Non-orthogonal die ▪ More die/wafer
Cost savings	▪ 2.1 µm/min ▪ 40 min vs. 2-3 hrs/wfr

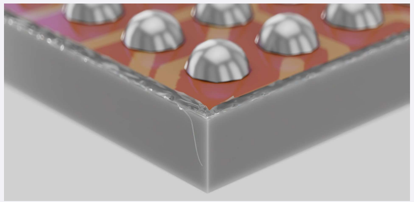


Defect Inspection to Verify Clean Die Edges

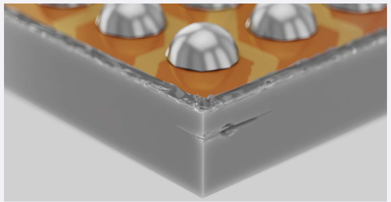


- Post-dicing die screening:
- 6-sided inspection for identification of process issues
- (Si use case shown)

Edge crack



Edge chip



Maintaining SiC die integrity with specialized process and process control

Bare Die Test Escapes Lead to Expensive Module Scrap

SiC Multi-Chip Module: Modeled Scrap Rate*

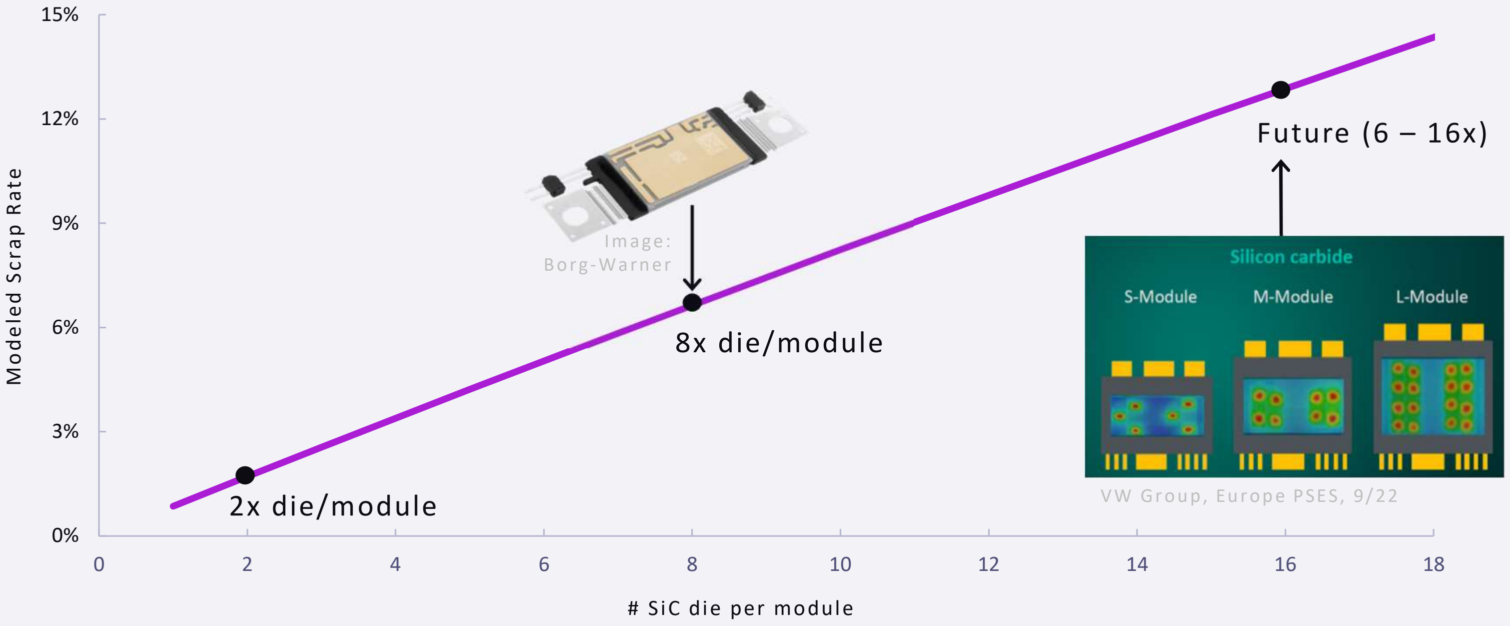


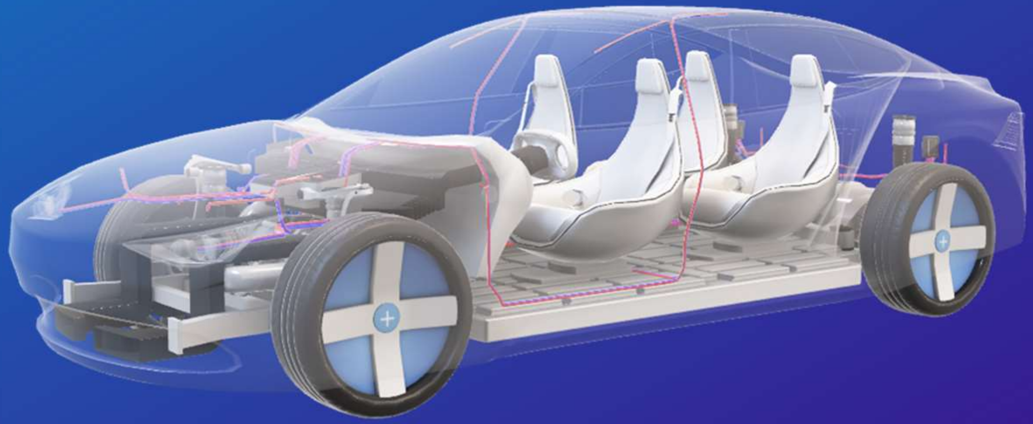
Image: Borg-Warner

VW Group, Europe PSES, 9/22

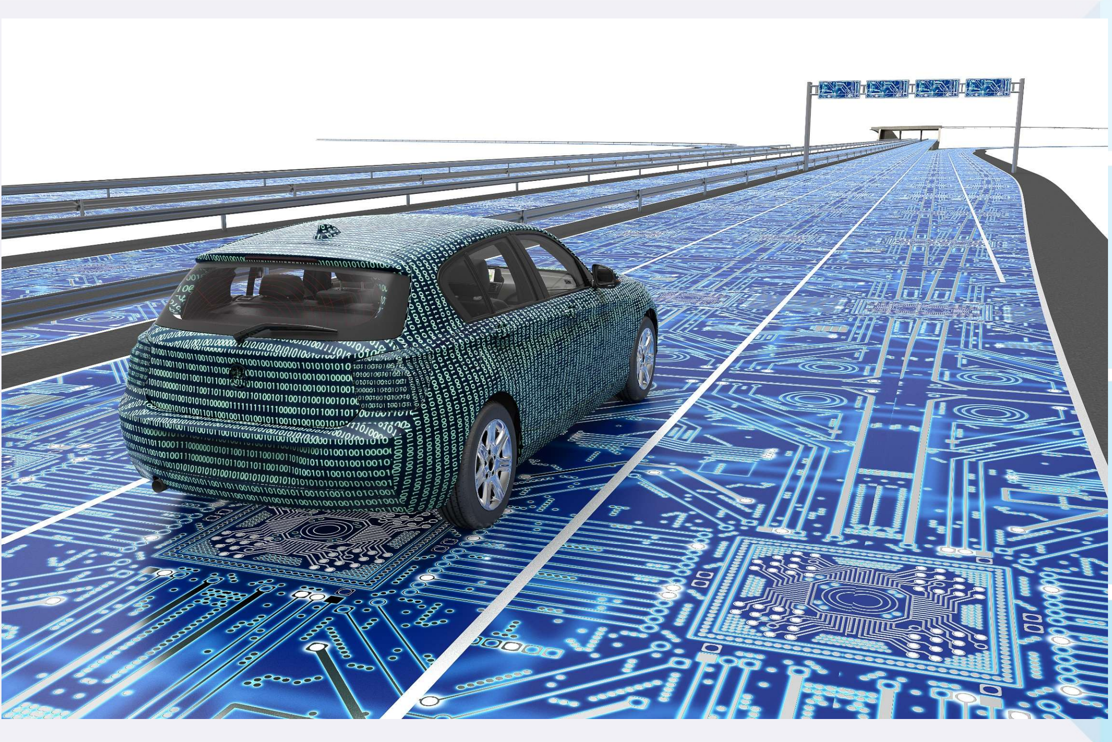
*Assumes 98% bare die test coverage, 65% bare die fab yield, W-B escape model. Projected scrap rates assuming the same escape rates as 2020.

Increasingly important to identify bad die at fab-level

Summary



Summary



The automotive industry has been forever changed by the chip shortage, vehicle electrification and the software-defined vehicle.

KLA works closely with the automotive ecosystem to develop a comprehensive portfolio of process control solutions.

The rise of SiC power semi devices poses additional yield, reliability, and cost challenges.

Inline defect screening is being adopted by automotive fabs to reduce escapes for reliability sensitive devices.

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Keep Looking Ahead