



# CHIP START | UK

the semiconductor incubator

managed by [SiliconCatalyst.UK](https://siliconcatalyst.uk)



Funded by  
UK Government



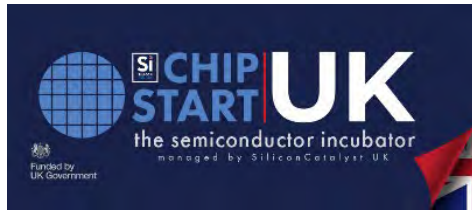
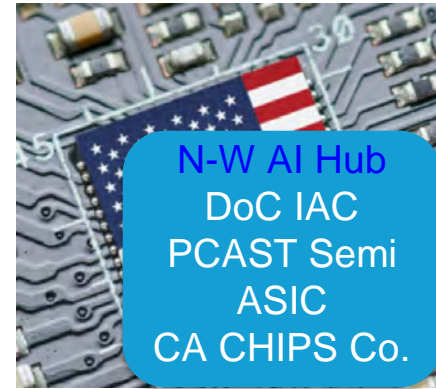
# UK Government funded semiconductor startup incubator



- Deploying Silicon Catalyst proven ecosystem for semiconductor startups
  - Training and advising
  - Free EDA tools, Design IP & Foundry from In Kind Partners
  - Links to the global semiconductor supply chain
  - Accessing and de-risking investment
- 9-month Semiconductor incubator
  - Fully funded by UK government
- Applications open [www.siliconcatalyst.uk](http://www.siliconcatalyst.uk) for Cohort 2
  - closing April 12<sup>th</sup>



# Ecosystem Centered on Startups



**International**  
UK, Israel & US Teams  
Advisors worldwide



**35+ Universities**  
STANFORD UNIVERSITY, HERIOT WATT UNIVERSITY, Berkeley UNIVERSITY OF CALIFORNIA, MIT, TEL AVIV UNIVERSITY, UNIVERSITY OF TORONTO

**Industry Partners**  
GSA, SITA SEMICONDUCTOR INDUSTRY ASSOCIATION, semi, PitchBook, nmi Semiconductors to Systems, VENTURE UNIVERSITY

**Accelerators**  
octane, PRAXIS CENTER for Venture Development, BATCHERY, INNOVATION SPACE, NEXTCORPS LUMINATE, KNX STARTUP

Good for Startups, Partners, Investors, Advisors ... the industry

# arm

Enter for a chance to win up to \$250,000 Arm Technology Credit

Arm Flexible Access for Startups Contest



Subject to Terms and Conditions

arm +



SECQAI

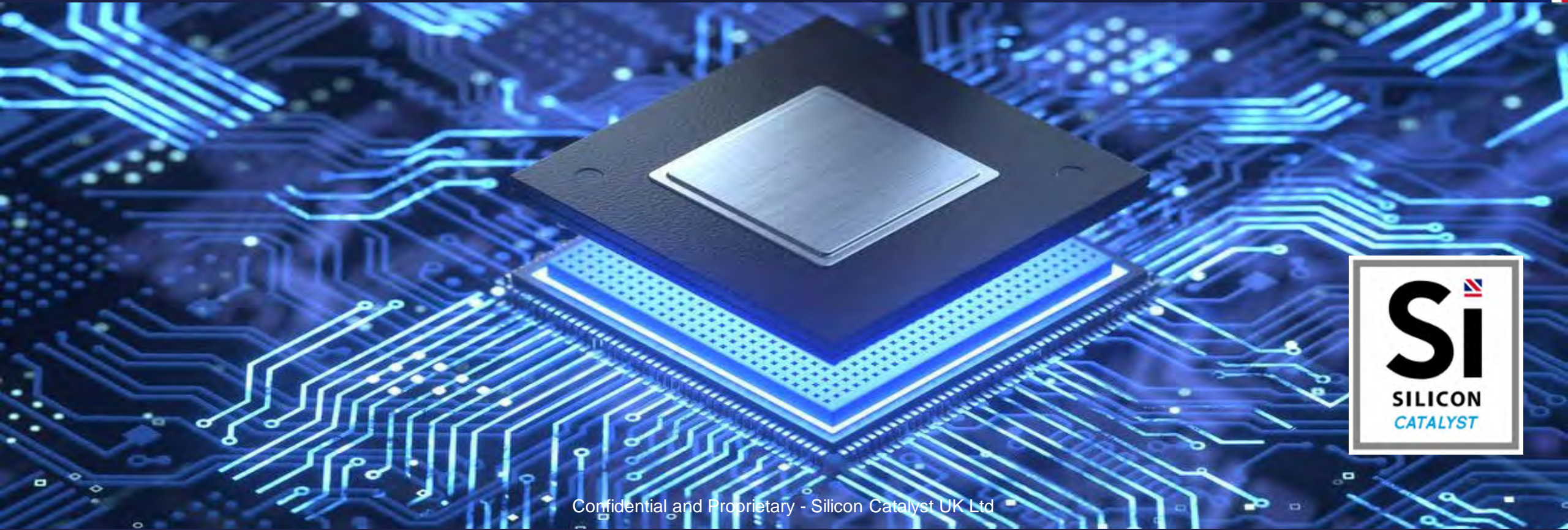
Rahul Tyagi  
CEO



Funded by  
UK Government

**Si** **CHIP** **START** | **UK**  
SILICON CATALYST

the semiconductor incubator  
managed by SiliconCatalyst.UK





# SECQAI

Confidential Computing with  
Post-Quantum Encryption

GSA London 2024

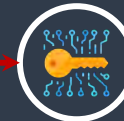
Confidential © SECQAI LTD.

# Our System on Chip simplifies and solves core customer problems

## Core customer problems needing to be addressed

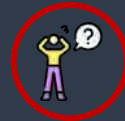
## SECQAI's 'Q-Locked' SOC: The "Apple" for security

Not prepared for the Quantum Threat



Post Quantum Cryptography & QRNG

Security is hard



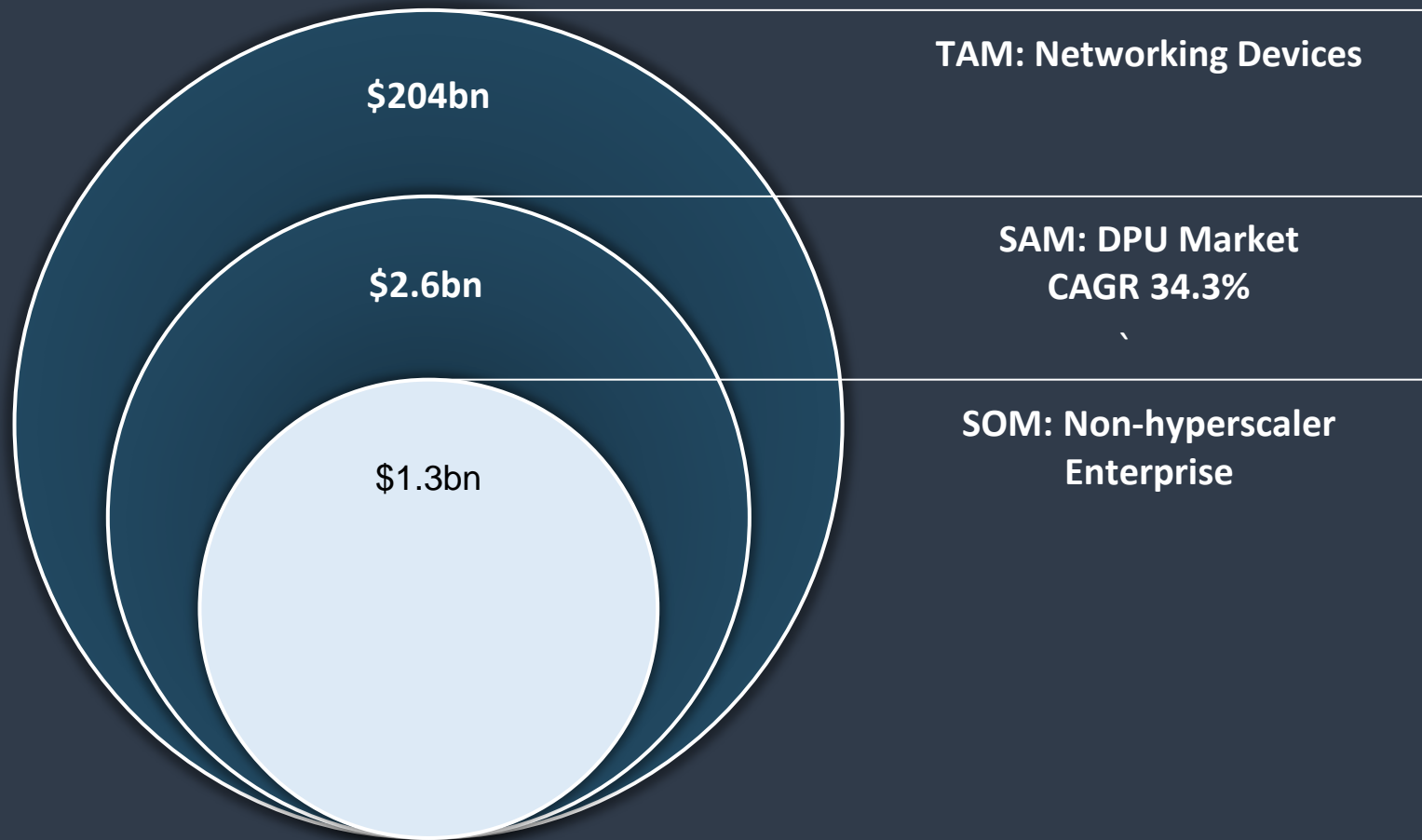
All your security tools, built in

Difficult and risky to compute at the edge



Memory safety for confidential compute

# Our focus will initially be on the DPU market



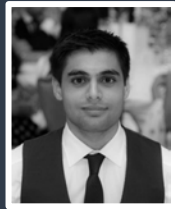
- Initial focus on Network Interface Card (NIC) / Data Processing Unit (DPU) commercial customers
- Firewall, XDR and cryptography functions are being offloaded to these devices
- Our strategy is to focus on user experience to gain traction: we target the neglected enterprise customer



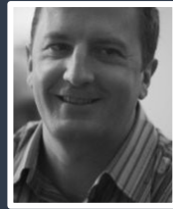
# Leadership



Angus Lockhart  
COO



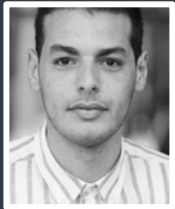
Rahul Tyagi  
CEO



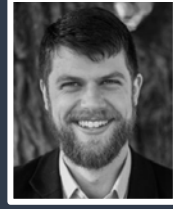
Graham Harris  
CFO



Andrew Addison  
Firmware



Alaeddine Jendoubi  
Photonics  
Hardware



Andrew Nicol  
Hardware  
Engineering Lead

... of a team with experience from leading organisations



# Come & have a chat!

1

Helping you bring Post Quantum Cryptography to your products

2

Scaling up the impact we can have through an investment round soon

# SECQAI

Interested in discussing further?

[contact@secqai.com](mailto:contact@secqai.com)

[www.secqai.com](http://www.secqai.com)

Tuesday, 12 March 2024

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# Vaire Computing

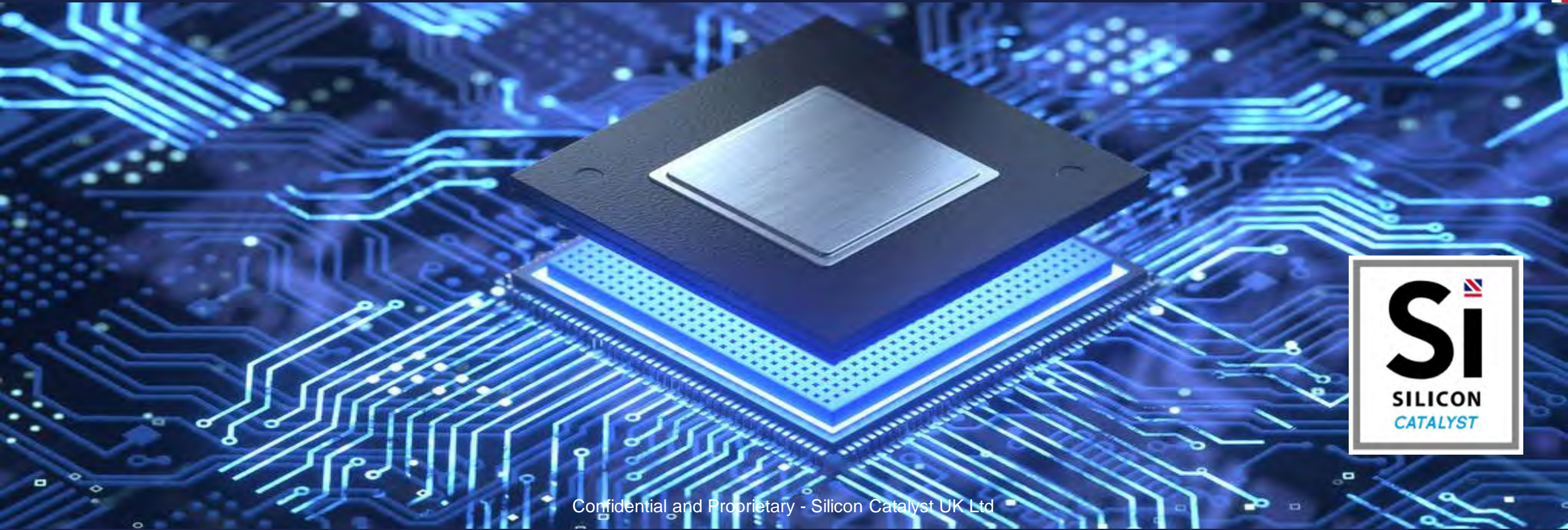
Rodolfo Rosini  
CEO



  
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UK Government

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the semiconductor incubator  
managed by SiliconCatalyst.UK



**Rodolfo Rosini**  
**CEO & co-founder**



Near-Zero Energy Chips for Generative AI

# Everyone else is wrong

- There is no point investing time and resources in anything other than approaching sub-Landauer computing
- Incumbents keep running in the opposite direction, building faster and hotter chips

# The future of chips is Near Zero Energy

Vaire Computing, founded in 2021, working on NZECs

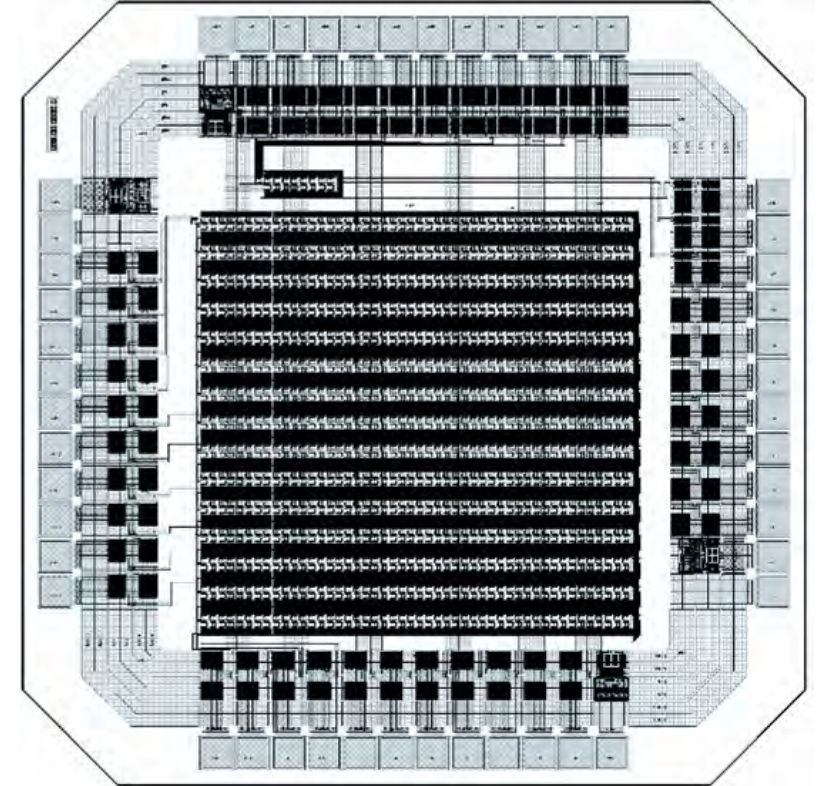
Team ex Acorn/Arm/Google/Neuralink/Imagination/AMD

Raised \$4m in seed funding from UK/US VCs

In discussions for a significant Series A in Q4 2024+

Initial market is always-on AI for IoT /  
defense / data centers

Test chip in 2025, mass market in 2027



# **We are hiring!**

**London, Cambridge, Seattle, Sunnyvale**

**Multiple openings:  
Engineering, Product Management, Comms, Ops**

**Looking for high-intensity world-class performers**

**RODOLFO@VAIRE.CO**

# HyperCIM

Tanyaradzwa Mangoma  
CEO



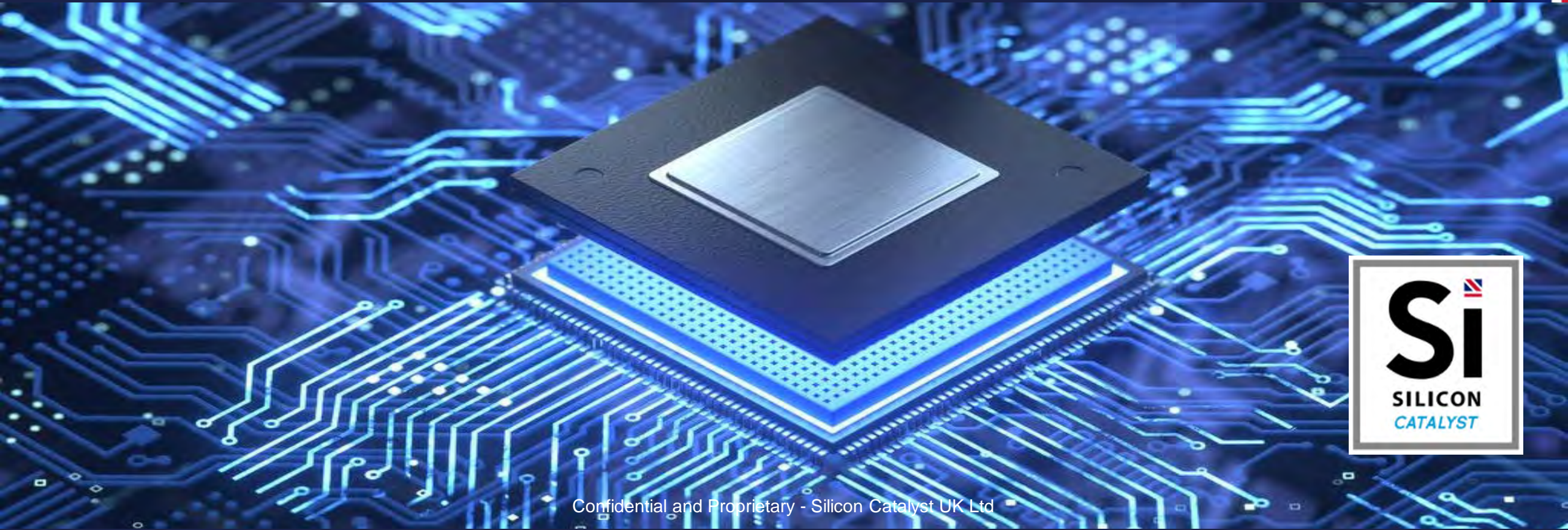
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# HyperCIM

Empowering | Enterprise | Software | Efficiency

**Dr Tanya N. Mangoma**

Founder

[tanya@hyperCIM.com](mailto:tanya@hyperCIM.com)

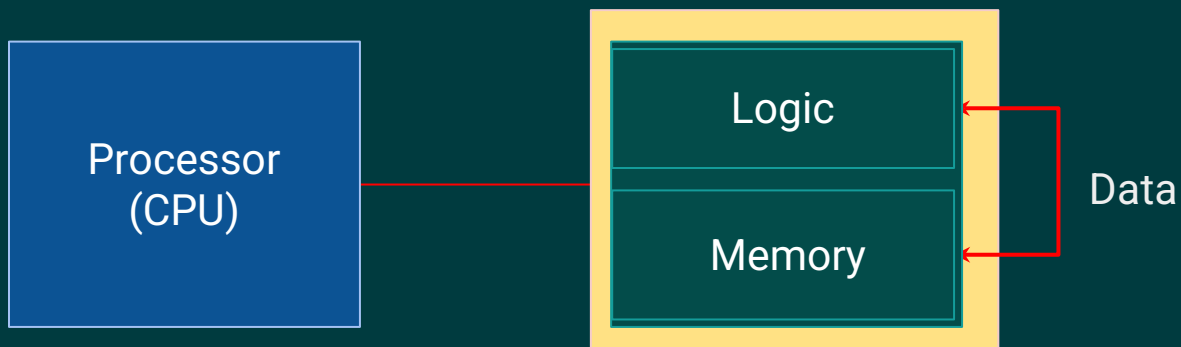
HyperCIM.com

# Compute-in-Memory: Cut power and execution time by processing data where it is stored.

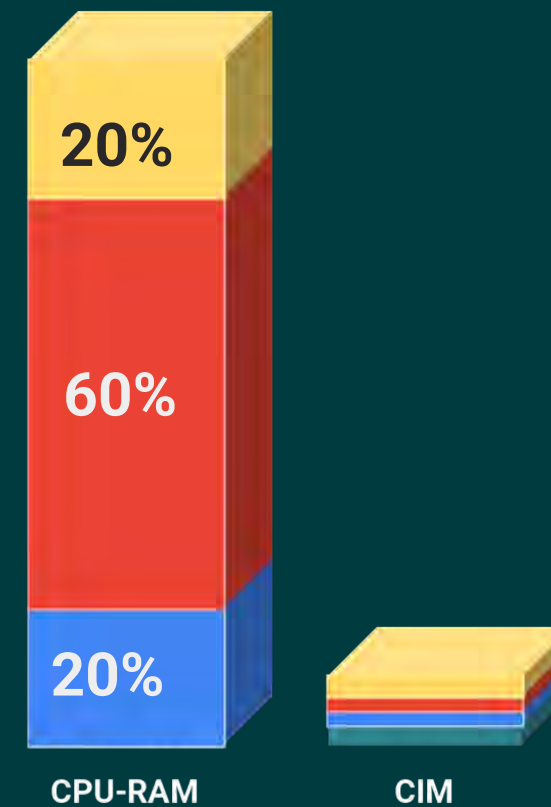
## Current Bottlenecked Execution:



## HyperCIM's Compute-in-Memory Co-Processor:



■ RAM ■ Data Movements ■ CPU  
■ Compute in Memory (CIM)



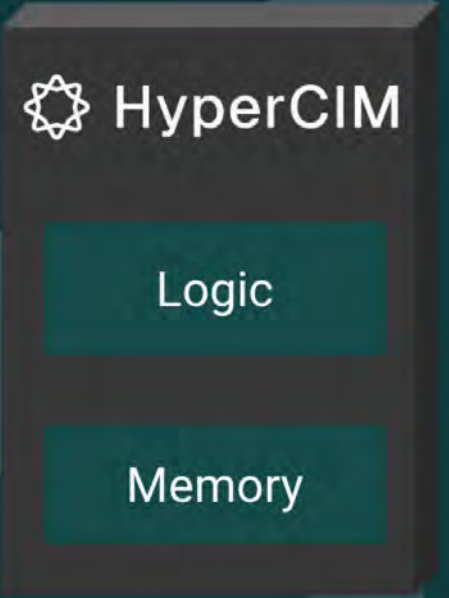
10x

Performance Improvement

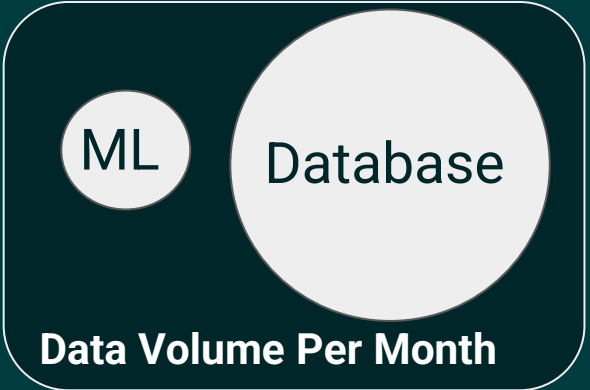
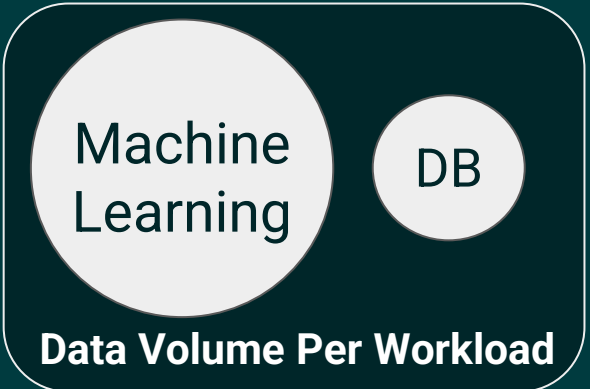
# Made for Enterprises: Fastest co-processor for real-time database applications.

## Product

GTM ODM:  
Foxconn  
Quanta  
Supermicro



## USP



## Market

### TAM

USD \$80 B

### SAM

USD\$55 B

### SOM

← USD \$1B

- E-Commerce
- Finance & Banking
- Streaming Services

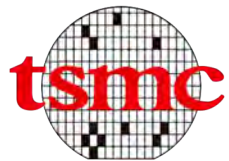
# Ecosystem Integration: Ensuring compatibility with existing processes



## Incubated by:



## Vendor Partnerships (NDA Stage):



Memory IP  
Chip Tapeout



Foundry Interface  
Design Services



Peripheral SoC IP

**Dr. T. N. Mangoma**  
Expert in Emerging Computing  
Hardware



## Advisors

**Dr. Ashraf Lotfi**  
Exited Semiconductor Founder  
(Altera, Intel)



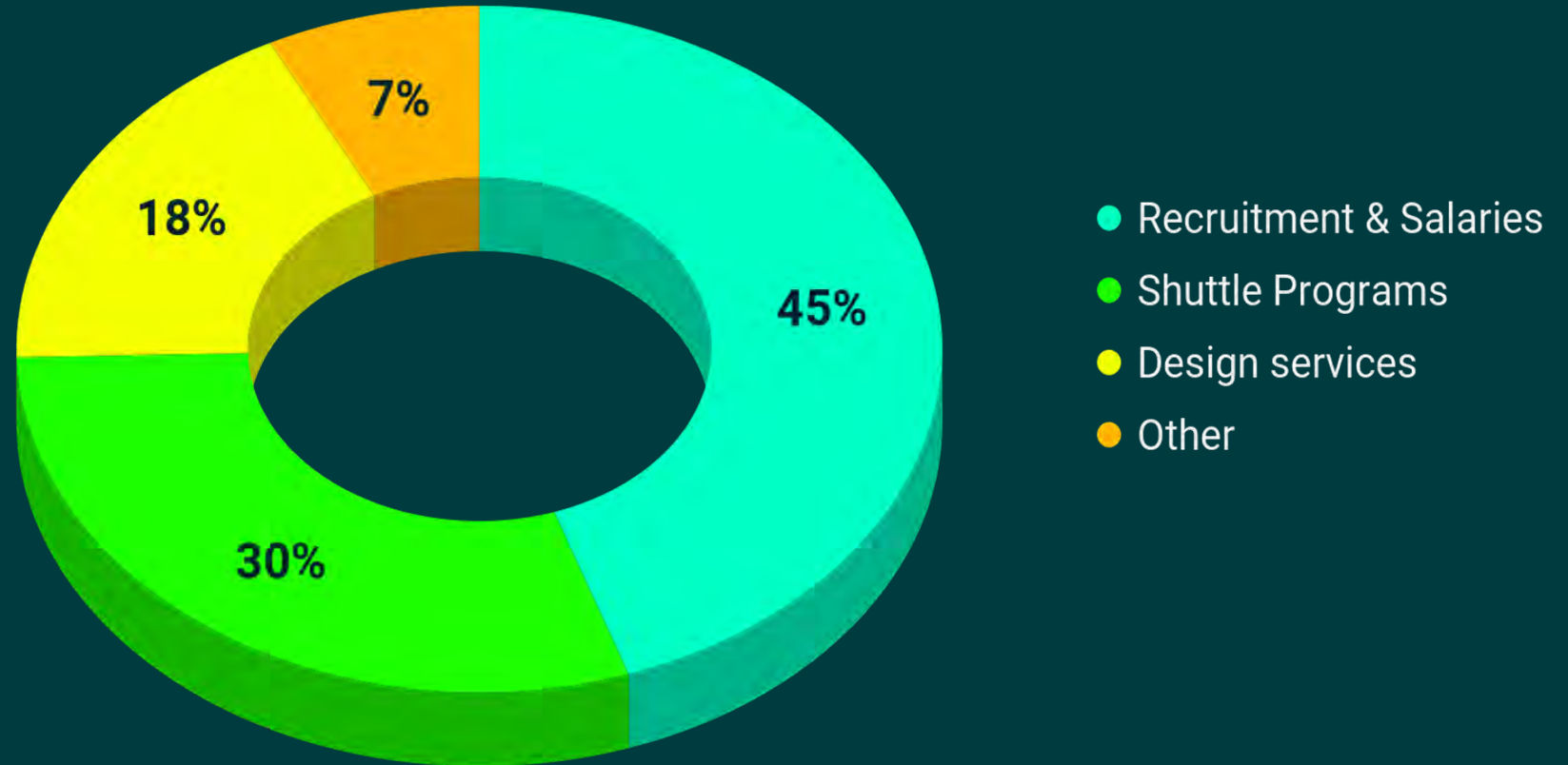
**Jamie Urquhart**  
Co-Founder of ARM



**Dr. Brock Doiron**  
Enterprise GTM, Software Interface



Seed funding requested:  
£3.3M for Q3 2024



Get in touch: [tanya@hyperCIM.com](mailto:tanya@hyperCIM.com)

# RED Semiconductor

James Lewis  
CEO



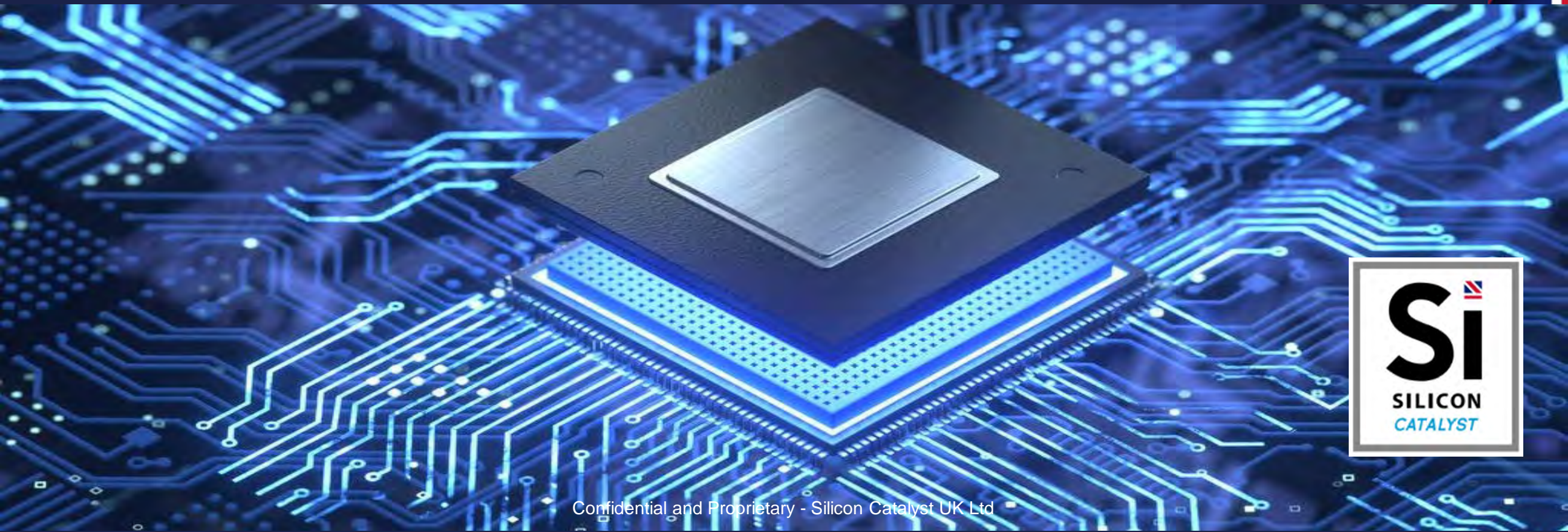
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# VISC

## Versatile Intrinsic Structured Computing

**All the benefits of hardware acceleration – All the versatility of a Microprocessor**

Algorithmic microprocessor architecture transforms performance  
for Edge AI, Autonomy & Cryptography

**James Lewis**

Chief Executive Officer

[james.lewis@redsemiconductor.com](mailto:james.lewis@redsemiconductor.com)

+44 (0)7903 849974

# New compute for exponential demands

## Why?

AI, Cryptography,  
Codecs, Autonomy...



- Increasing algorithmic compute demands
- Soaring power consumption
- Massive design complexity
- Spiraling up cost of silicon

## What?

VISC IP Core innovation  
delivers:



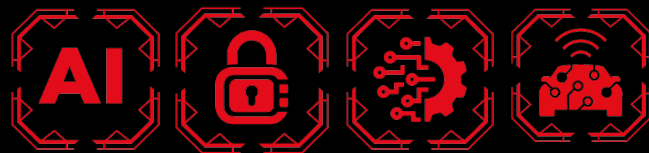
- 10 - 100x maths performance boost
- Best maths-per-watt power
- Security of critical data
- Most efficient use of silicon area

## Our product

Innovative IP defensible by patents –  
licensed to customers:



- Reconfigurable execution architecture
- Optimises for parallelism in real time
- Holistic algorithm sequencing
- Memory efficiency ... no memory accesses during computation
- Simple 'Reconfig' instructions for any ISA



DCT

FFT

Matrix  
Multiply

Trigonometry

Logic

Non-linear  
Problems



# Highly experienced team addicted to changing the Future of Microprocessors



**CEO**  
James Lewis

Tech Starter and Builder  
Oxford Semiconductor (sold to Kioxia)  
Redux Labs (sold to Google)



**Technical Strategy and Governance**  
David Calderwood (Director of R&D and Chair)  
Chartered Engineer and team-builder



**Product Development**  
Andrey Miroshnikov (Senior Eng)  
Qualcomm



**Commercial Strategy – Winning Customers**  
David Harold (COO)  
Imagination



**Product Development**  
Shriya Sharma (Embedded Eng)  
Southampton Uni



**Industry Expert**  
Steve Evans (Advisor)  
Arm, MIPS, Imagination

**Expert advisory team**  
James Tout (Semiconductor Design) Kioxia/Oxford Semi  
Haydn Povey (Cybersecurity) ARM, IAR, IoTSE  
Justin Hill (IP) Dentons

Talent, Functions and Sector Experience to get the job done

# Taking our IP to market

## Market size and shape

## Business model

## Routes to market

## Target customers

TAM

Global microprocessor market in 2030:

**\$100 bn+**

SAM

No. of RISC-V chip implementations in 2030 world-wide:

**16 billion units**

SOM

RISC-V chip implementations in 2030 – Edge applications in accessible territories:

**6.6 billion units**

License and royalty revenue for VISC Core IP

Established business model for microprocessor IP-creative companies

Partnerships:

- IP Suppliers
- EDA tool vendors
- Design Services

Direct to Customers

Game-changers and leaders developing SoCs:

Fabs and Fabless Chip Companies

Microprocessor companies

### Today:

- Software sims => FPGA demonstration by RISC-V acceleration
- Demonstrated 50x code reduction in cryptography algorithm vs. ARM and x86
- Funded by grants; patent protection underway

### Raising Seed Capital now:

- £3.5m (\$4.5m) will take us to first hardware implementation and development kits into our lead customers

# Singular Photonics

Shahida Imani  
CEO



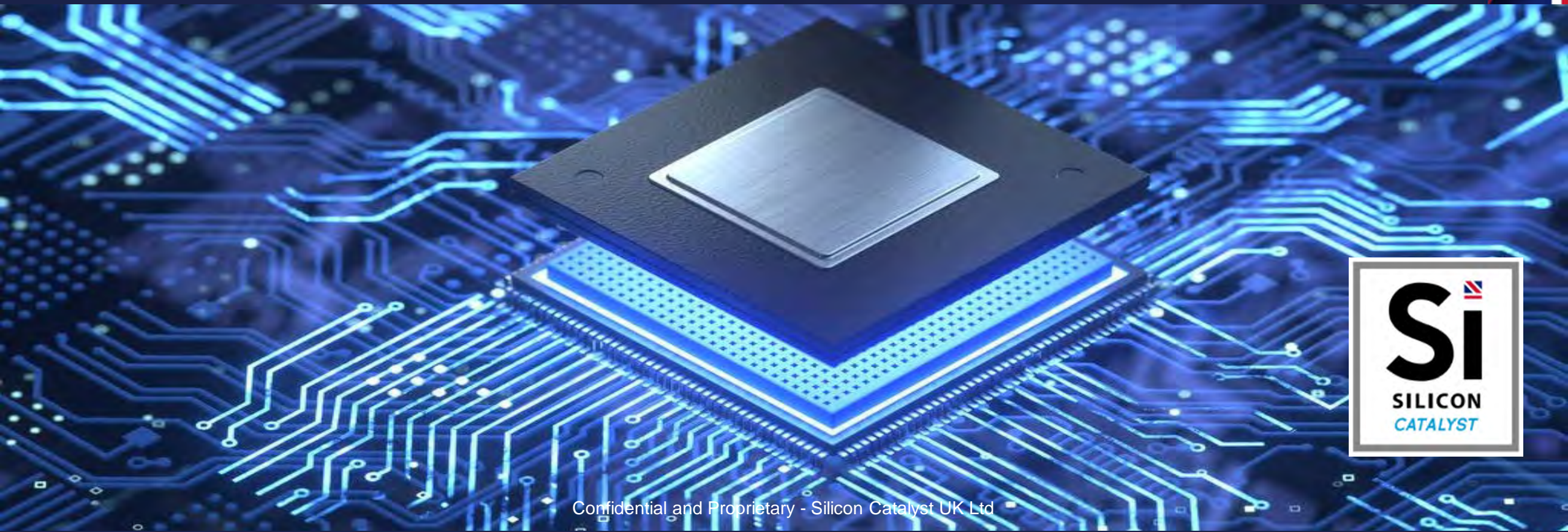
# CHIP START | UK

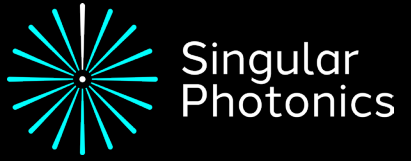
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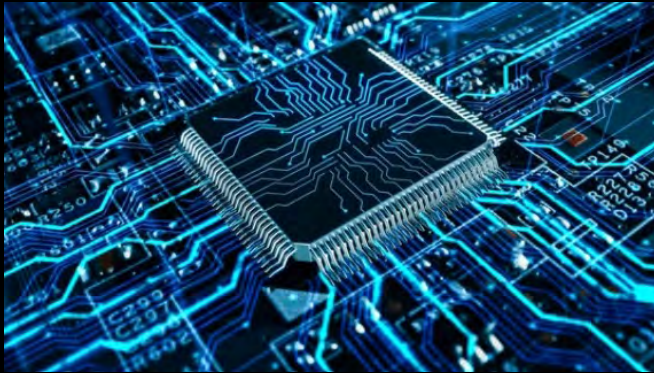
4D  
4D

# Introduction

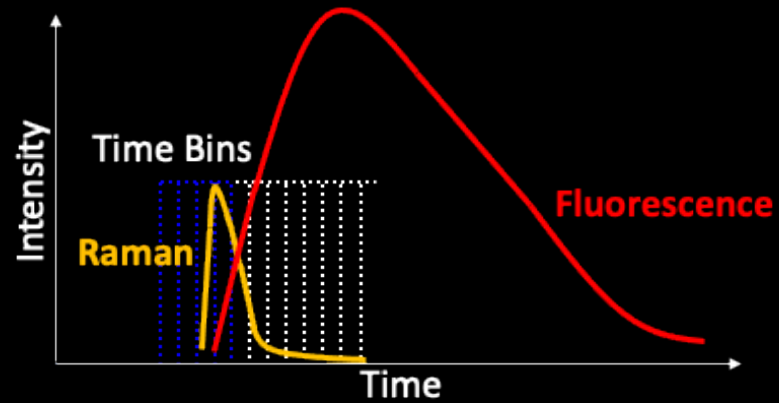
Imaging Time: The Fourth Dimension



## Imaging Time : The Fourth Dimension



**3D Stacked = 100% fill factor**

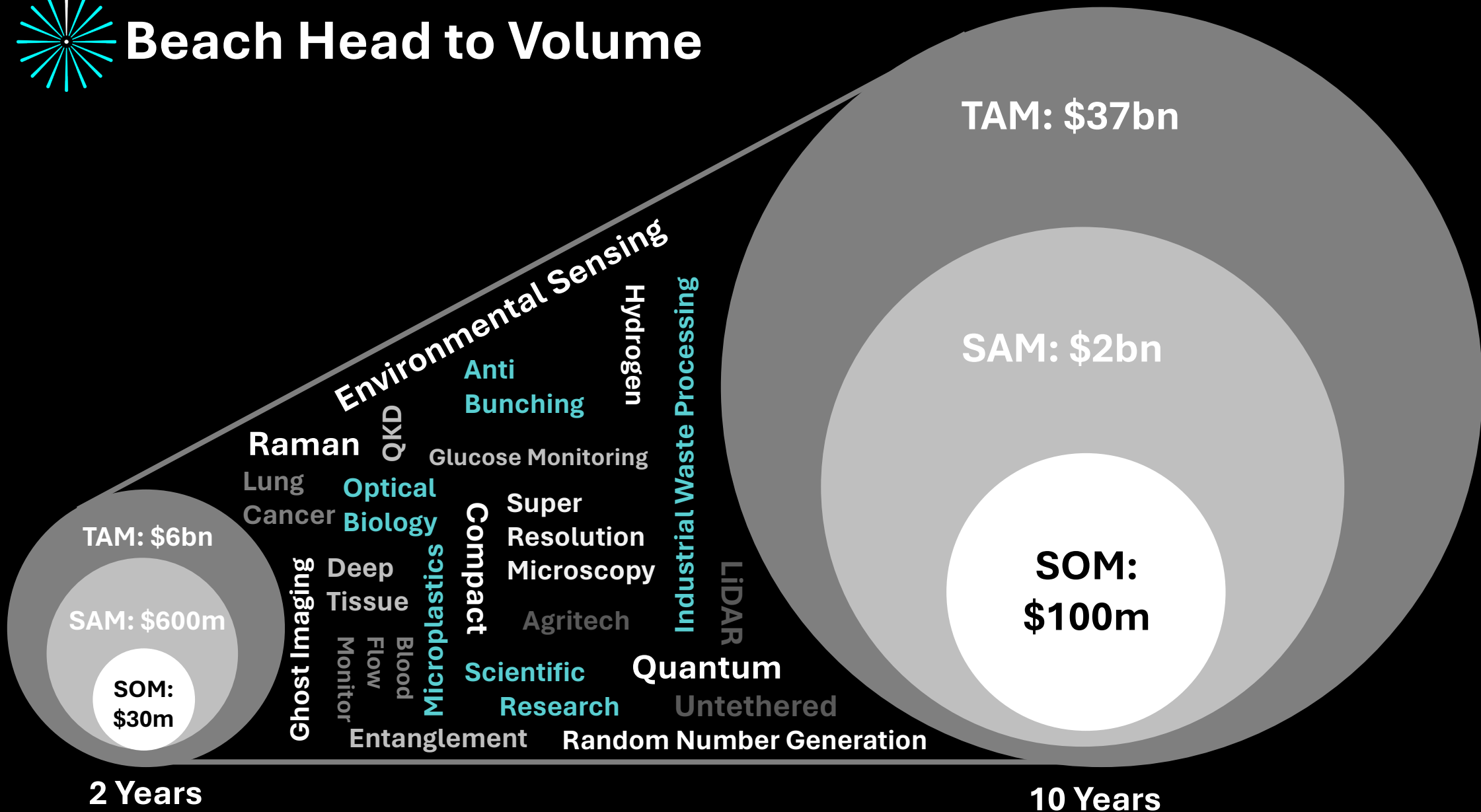


**Time binning every photon (4D)**

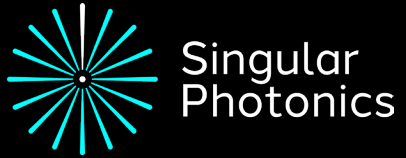
- Unparalleled **real time** pixel configurability
- **Detect 50% more** molecules
- **Low noise** and **low light** operation
- **Compact** form factor for handheld and mobile applications



# Beach Head to Volume



Beachhead: Scientific Instrumentation Market



## The Executive Team



### **Shahida Imani**

CEO / CFO and Co Founder  
Over 25 years experience in  
High Growth Technology  
Companies



### **Dr Aravind Jalajakumari**

CTO and Co Founder  
Sensor and electronics design,  
previous experience with ST  
Microelectronics

---

## The Non-Executive and Advisory Team



### **Pete Hutton** **Chairman / NXD**

Previous President of  
Product Groups, **ARM**  
Chairman Agile Analog



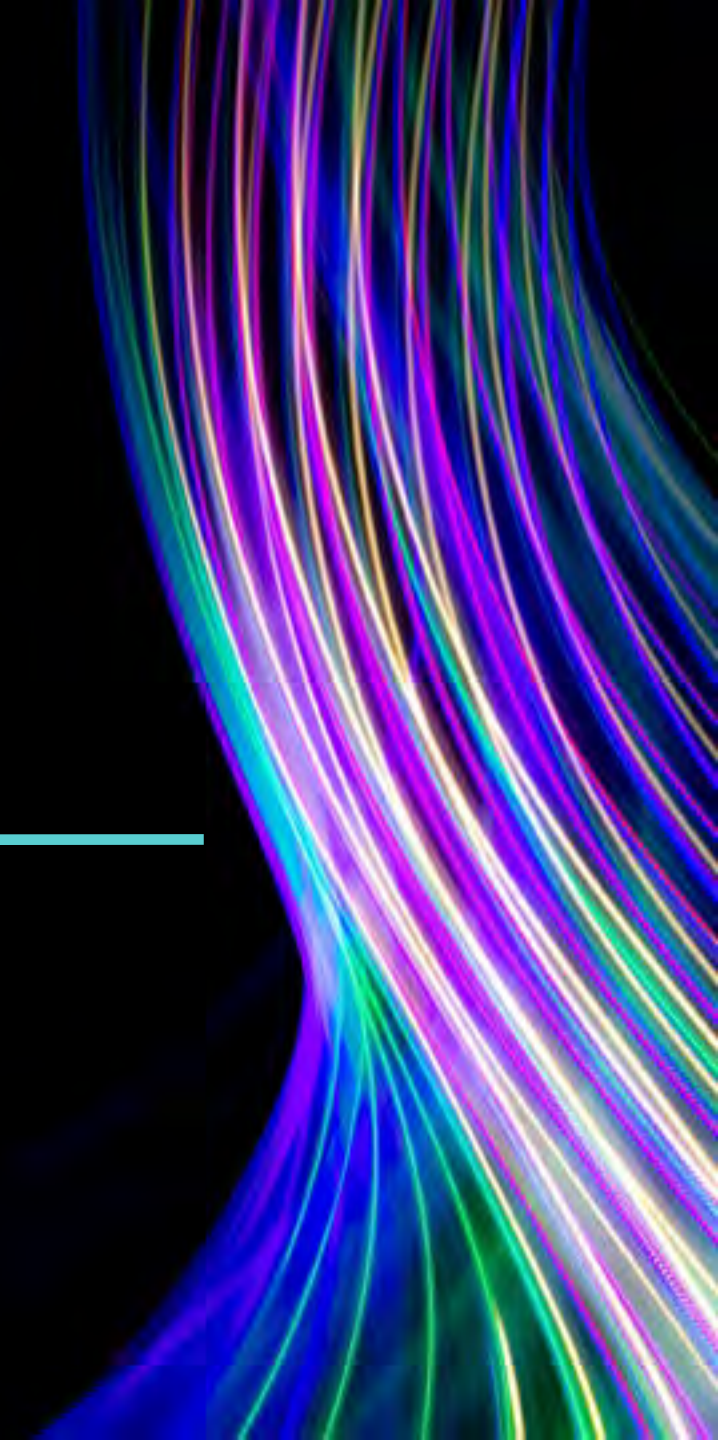
### **Prof Robert Henderson**

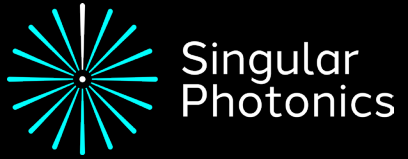
Chief Scientific Advisor & Co  
Founder  
World leading expert in SPAD  
sensor technology



### **Dr Neil Finlayson**

Applications Specialist and  
Co Founder  
Over 30 years' experience  
in ultra-fast optics





4D  
4D

Thank you & Questions



Shahida Imani  
CEO and Co- Founder  
[s.imani@singularphotonics.com](mailto:s.imani@singularphotonics.com)  
+44 7944 231537





# Blueshift Memory

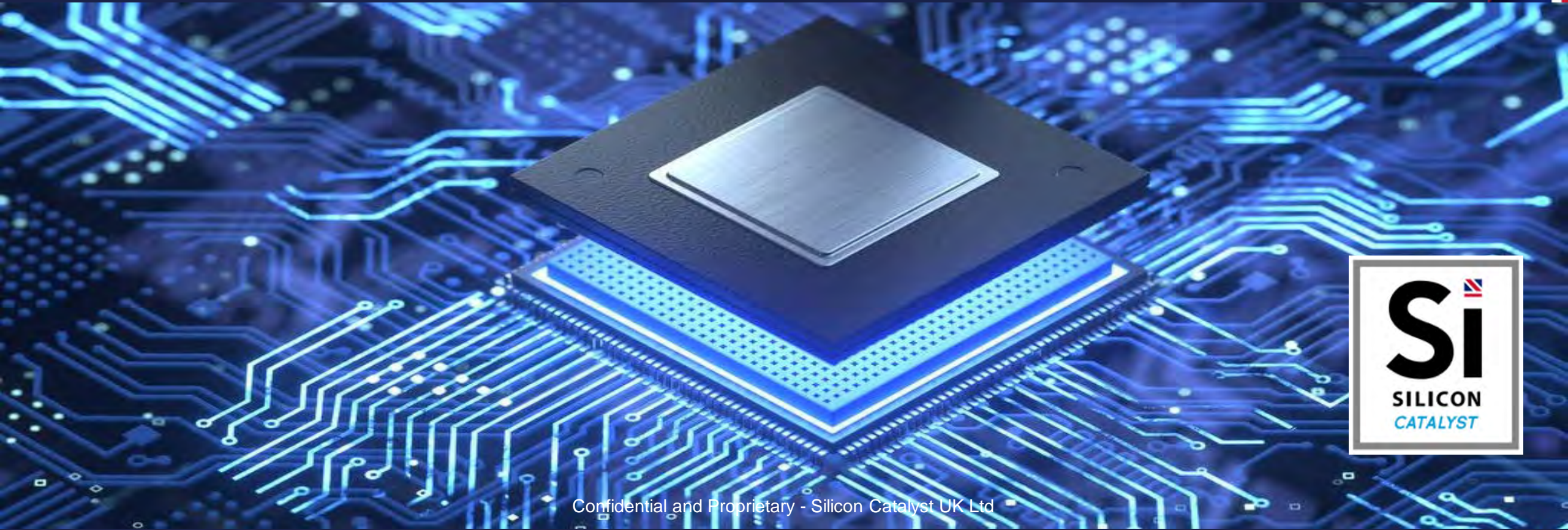
Helen Duncan  
Chief Marketing Officer



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# Blueshift Memory

Self-Organizing Memory

*Breaking through the Memory Wall*

Helen Duncan, Chief Marketing Officer

[info@blueshiftmemory.com](mailto:info@blueshiftmemory.com)

[www.blueshiftmemory.com](http://www.blueshiftmemory.com)



# Why Blueshift Memory?

## Our mission

To speed up  
memory-hungry  
applications without  
re-writing code

- AI/ML
- Data centers
- In-memory databases
- Automotive
- Mobile
- IIoT

## Overcoming the memory bottleneck

- ~80% of CPU usage is wasted handling data structure, rather than the calculation
- Self-optimising memory unlocks this performance

## Hardware-verified performance



**Zero**  
Latency

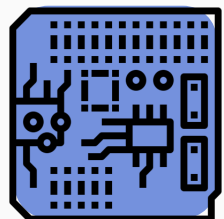


**300x**  
Speed



**-90%**  
Energy

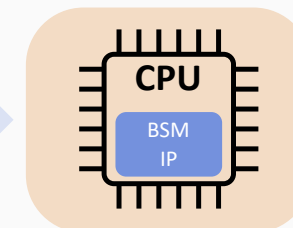
# Product and Market



FPGA



Chiplet



2024



2025



2027



The Market 2028



CXL-enabled Cloud



Chiplet-modified DIMM



DRAM and HBM





**Peter Marosan**  
Founder, CTO (Acting CEO)

**Patents: 5 Exits: 2**

Hungarian Academy of Science,  
Econet and UGS



**Guillaume d'Eyssautier**  
Lead Board Advisor

**Exits: 4**

Matra Harris Semiconductor,  
GEC-Plessey, Rockwell, IBM,  
Cadence, PicoChip and other  
startups



**Helen Duncan**  
CMO

Plessey 3-5, ROHM  
Semiconductor, United  
Business Media, Publitek



**Dr Theodore Omtzigt**  
Founder and Advisor

**Patents: 10**

NVIDIA, Intel, 3DFX and  
Stillwater Supercomputing



**Kitrick Sheets**  
Founder and Advisor

**Patents: 7**

Cray, Supercomputer Systems



**Dr Sarmad Adeel**  
Senior Embedded Engineer

Hamburg University of  
Technology (TUHH), NXP  
Semiconductors



**Sarah Bayliss**  
Finance Manager

Harting UK Limited

## Advisors

**Dr Ron Black:** *CEO Codasip*  
**Rupert Baines:** *CEO QPT*  
**Dr Audrey Stone:** *Legal/IP*  
**Allan Cattle:** *Open Compute  
Project Foundation*  
**David Stewart:** *ChipStart UK  
advisor*

MintNeuro

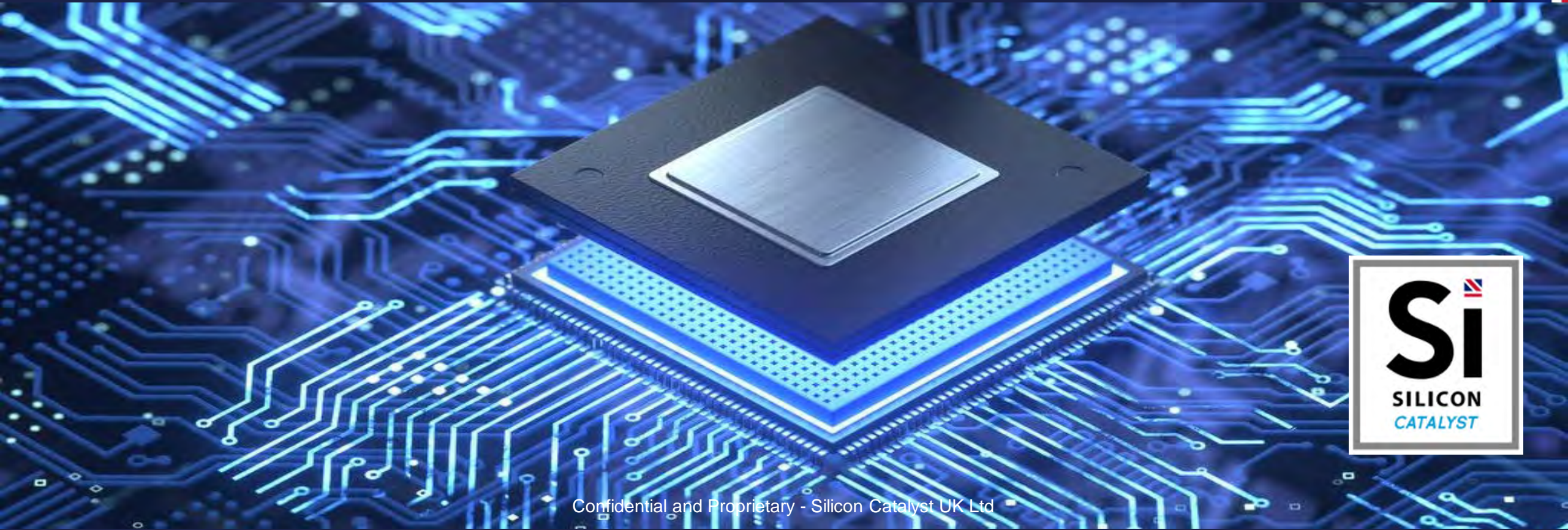
Dorian Hacı  
CEO



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# mintneuro

**Empowering next-gen neural implants**  
with advanced semiconductor technology

large expensive

invasive

outdated

**TODAY**

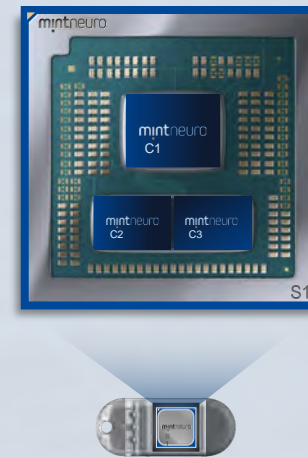
low performance

long time-to-market

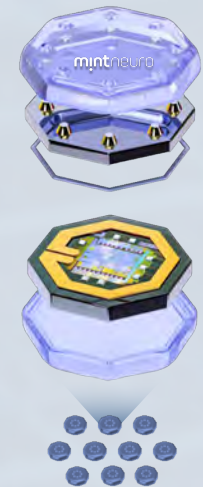
Integrated Circuits



Integrated Systems



Integrated Implants



**Efficient, compact,  
medical-grade devices**

**to enable scalable, less invasive,  
more accessible neural interventions**



Dorian Haci  
**CEO**



Tim Constandinou  
**CTO**



Andy Jackson  
**CSO**



Tim Denison  
**Chair**



Semiconductors

Neuroscience



Medical Devices

## Patent-protected intellectual property

SPINOUT FROM  
**IMPERIAL**



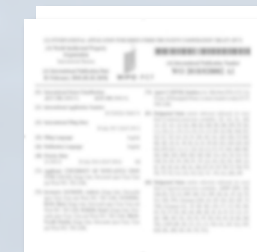
Implantable Neural Interface  
(granted in UK, US)



System for Brain Computer Interface  
(granted in UK, US)

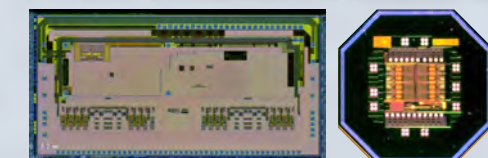
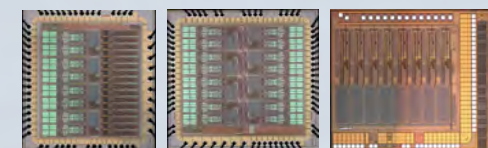
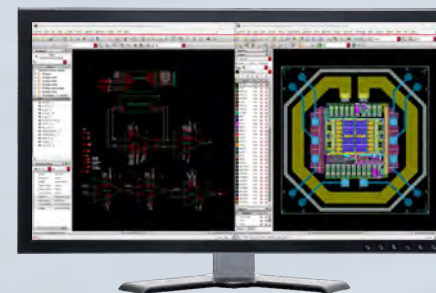
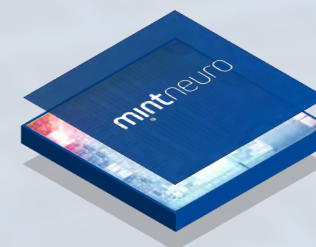


System and method for neuromodulation  
(granted in UK, US)



SiP architecture for neural chipsets  
(filing in UK, US)

## 12 years in neural chip design

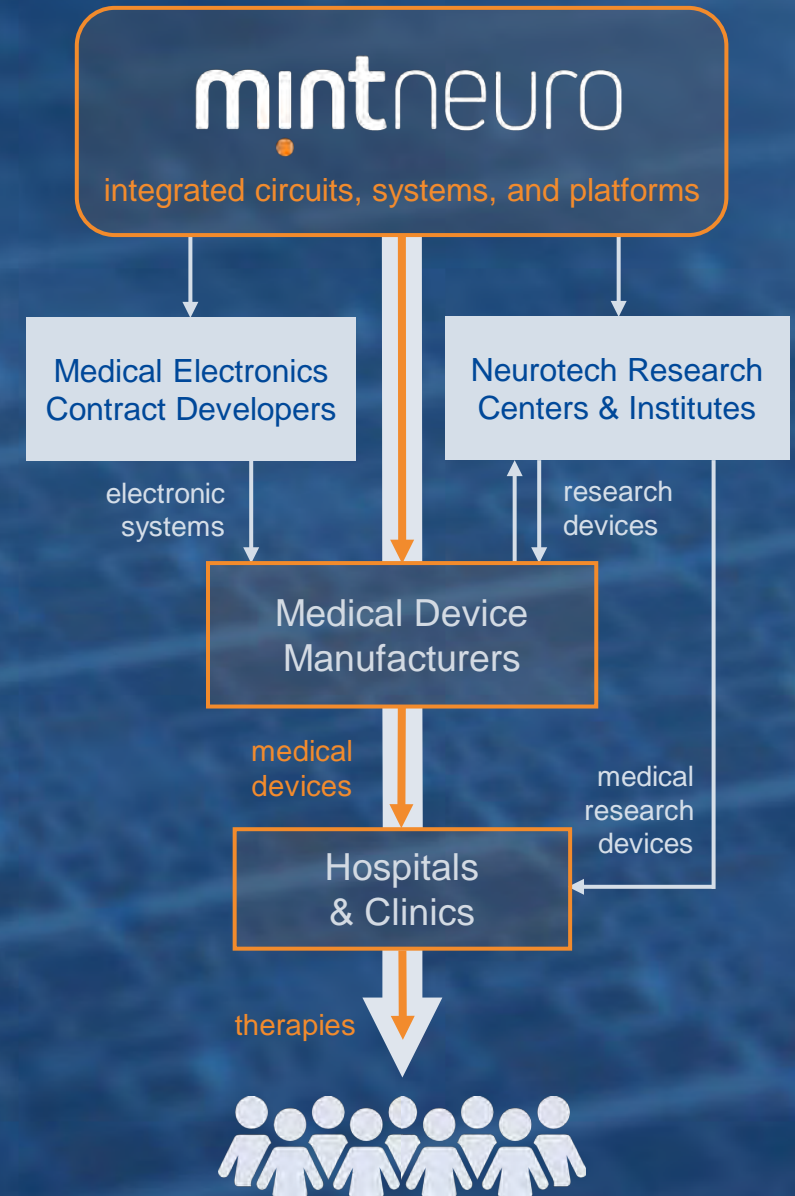
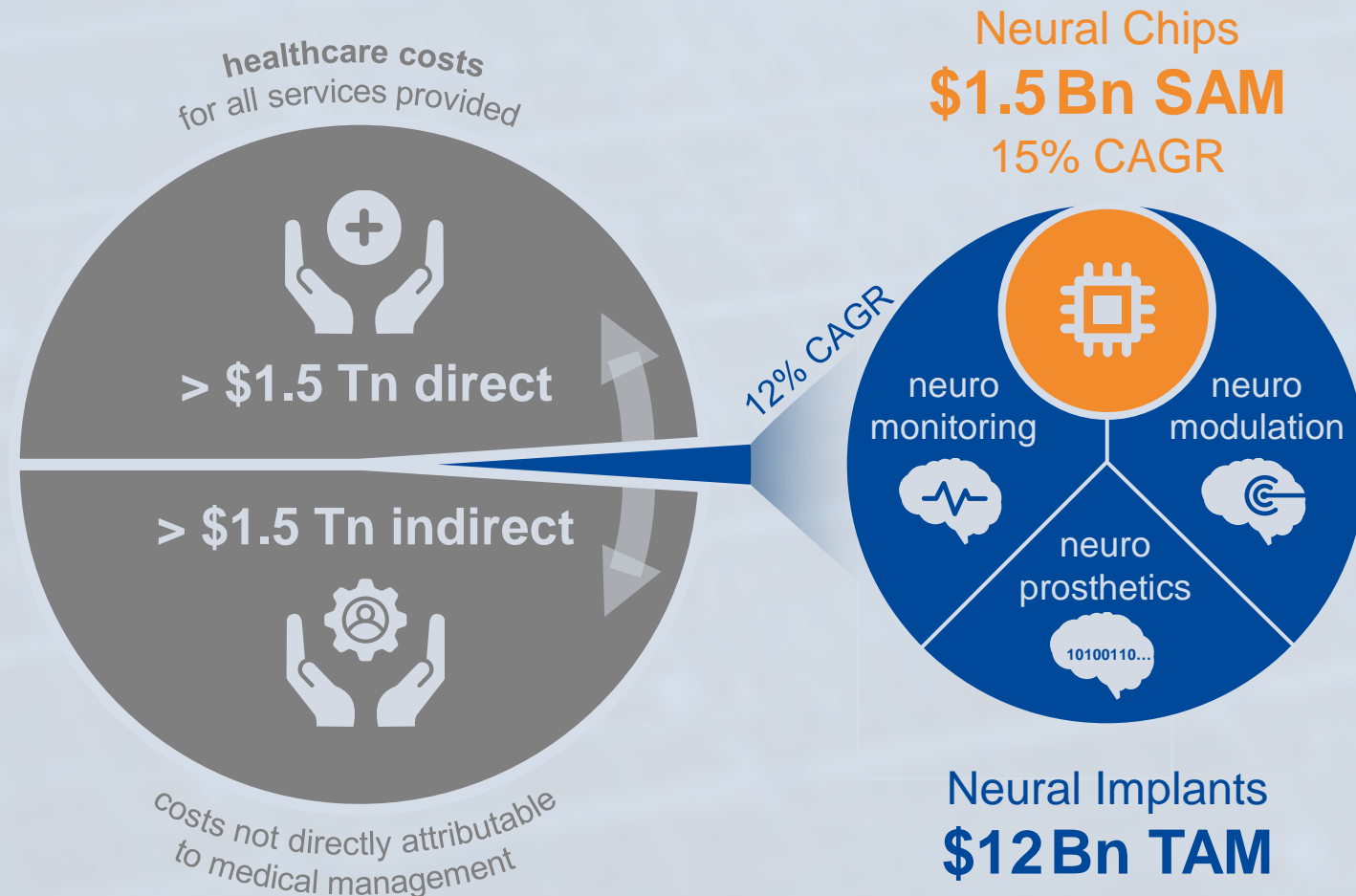




# Untapped market opportunity

“The total cost of neurological disorders is equivalent to the cost of heart diseases, cancer, and diabetes ... combined.”

– Economist Impact, 2020



# Wave Photonics

James Lee  
CEO

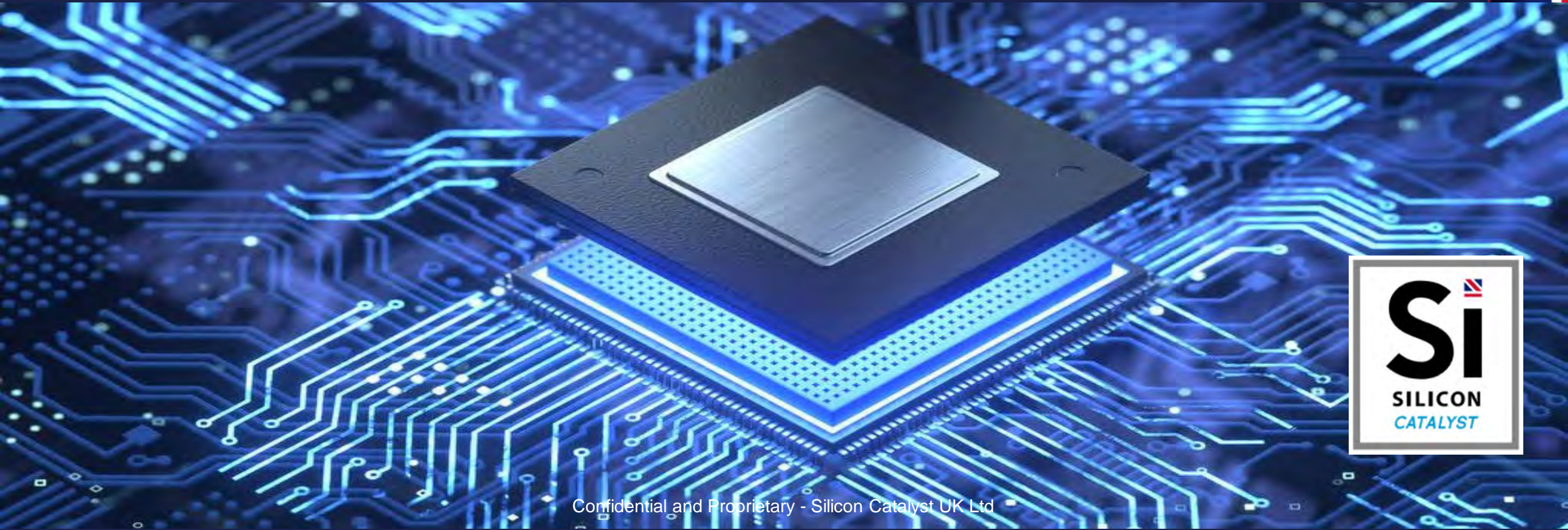


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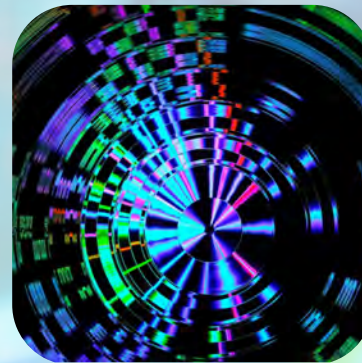
P H O T O N I C S

The platform for the future of photonics

# Integrated Photonics

**Driven by datacoms... ..but can unlock:**

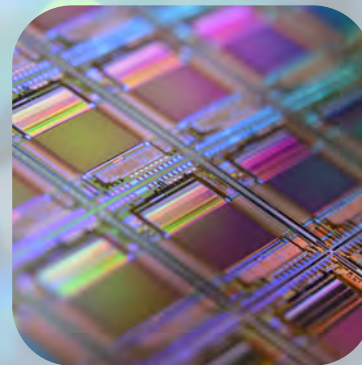
- Exploits \$100Bs of investment in semiconductor processing
- Leveraged to address demand for bandwidth and energy reduction in datacentres, HPC and AI model training



Quantum



Healthcare



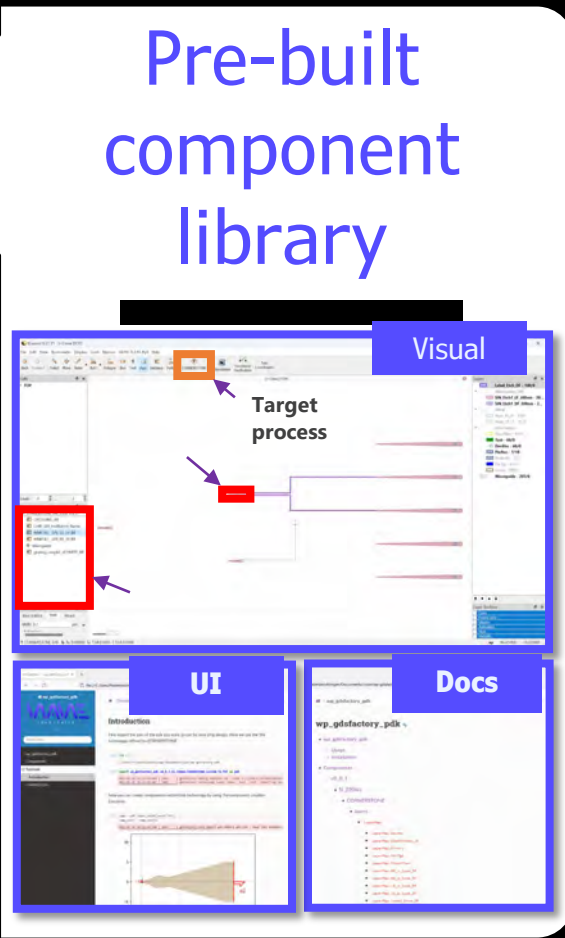
Optical computing



Lidar

# The opportunity – why Wave Photonics?

**Pre-built component library**



The screenshot displays a software interface with three main sections:
 

- Visual:** A central workspace showing a schematic diagram with a 'Target process' label and various components. A red box highlights a specific component in the left-hand panel.
- UI:** A bottom-left panel showing a user interface with a graph and text.
- Docs:** A bottom-right panel showing a document titled 'wp\_gdfactory.pkl' with a list of parameters and values.

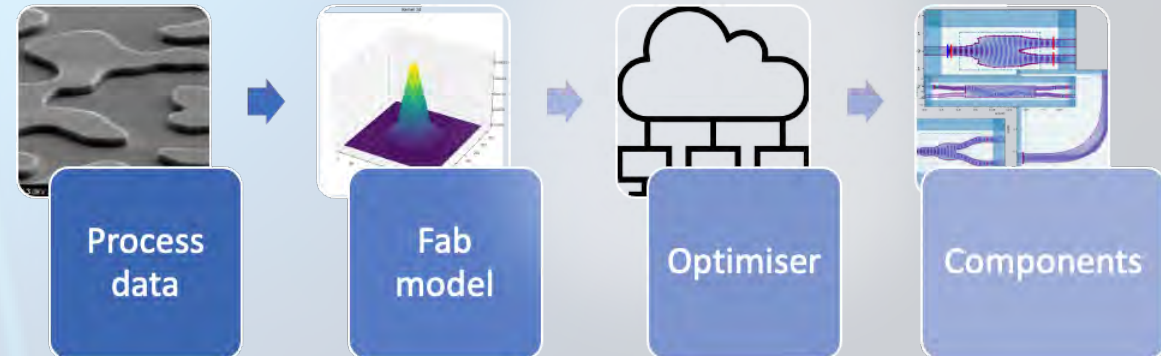
## From: Multi-year development



Inherently analogue design, sensitive to process variation

- Error-prone, iterative design

## To: Ready to go building blocks



# Team

## Founders



James Lee - CEO



Matthew Anderson - CSO



Mateusz Kubica - CTO



## Board/Advisors



Ming Zhang – Board Member



Mark Miller – Advisor



### Technical team

Team of 4 photonics engineers with experience across quantum photonics, chip design and optimisation



### To join

**Confirmed:** Advisor – commercial photonics background

**With seed round:** Product manager/BD, Project manager, integrations engineer/developer, simulation engineer

Literal Labs

Noel Hurley  
CEO



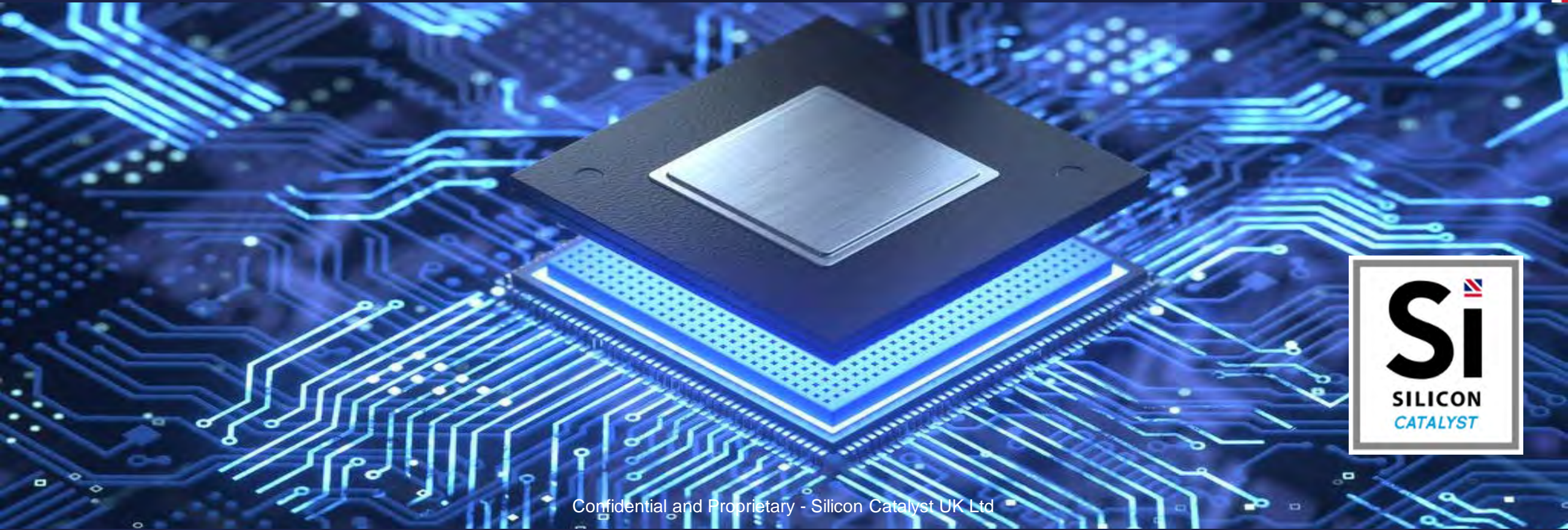
**CHIP  
START | UK**

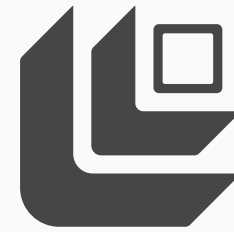
the semiconductor incubator

managed by SiliconCatalyst.UK



Funded by  
UK Government





**Literal  
Labs**

# A new generation of energy efficient AI

Noel Hurley  
CEO  
Literal Labs

[NOEL@LITERAL-LABS.AI](mailto:NOEL@LITERAL-LABS.AI)

[WWW@LITERAL-LABS.AI](http://WWW@LITERAL-LABS.AI)



A CAMBRIDGE FUTURE TECH VENTURE



# Literal Labs

AI based on Tsetlin  
Machines and  
propositional logic



## High Throughput

250x faster inferencing using  
software only on today's silicon

1000X when accelerated!



## Ultra Low Power

Logic not multiplication!

10,000x lower energy per  
inference can be achieved



## On chip training

Low compute complexity  
enables edge training



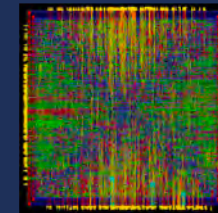
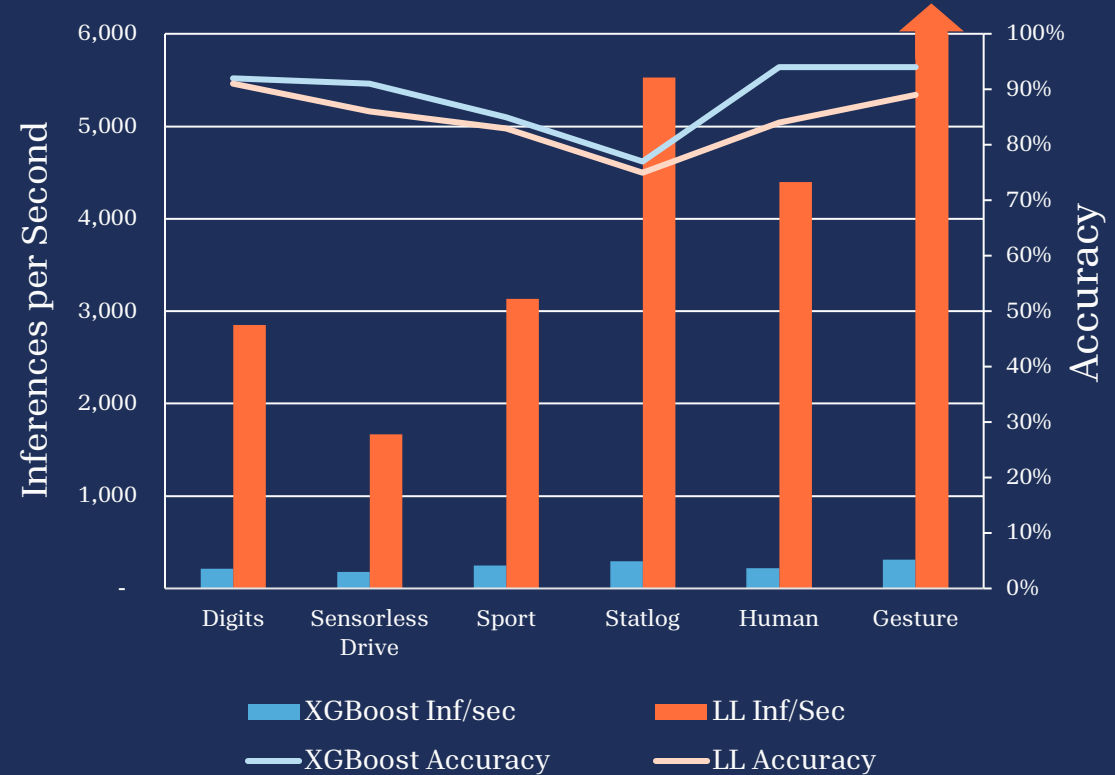
## Explainable AI

Our architecture enables  
explainability and ensures  
accountability for decisions  
made

# Benchmark Example

Same Datasets  
Same Hardware  
Published Optimised Results  
Benchmark papers available.

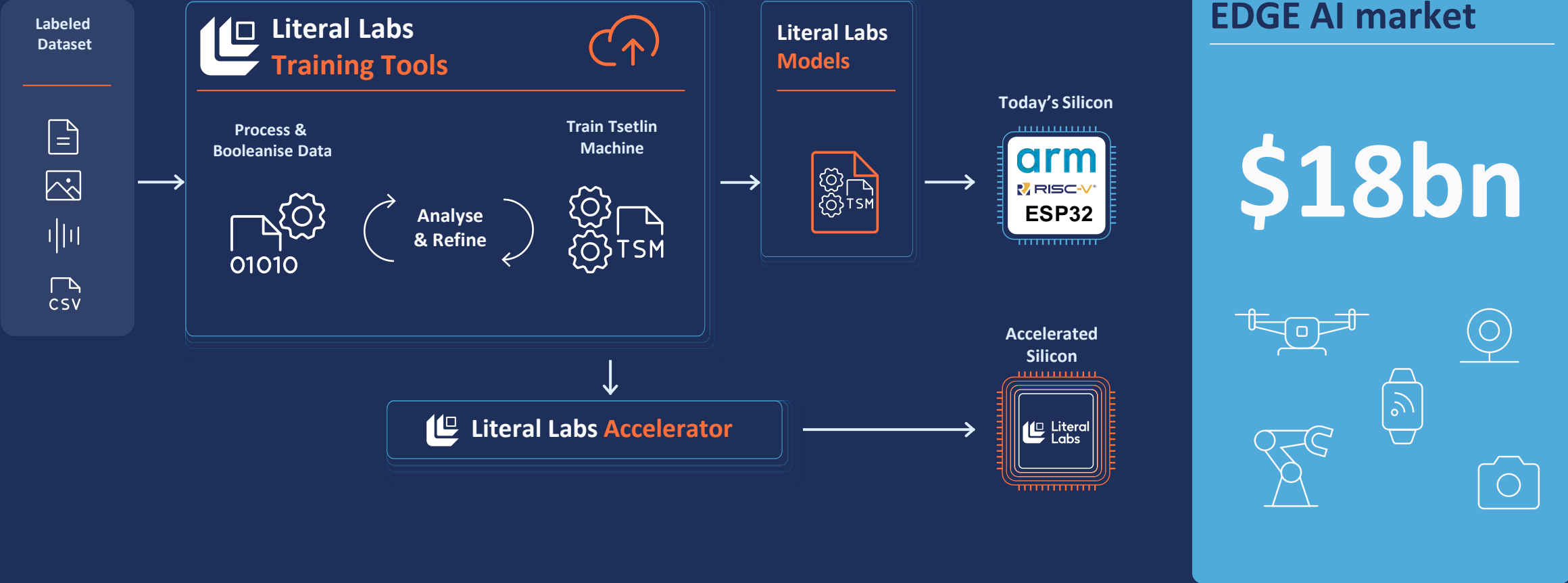
## Literal Labs vs XGBoost



Another 100x faster  
when Literal Labs  
accelerator present

# Literal Labs

## Product and Initial Market



# Our team

## Core Team



**Noel Hurley**

**Chief Executive Officer**

Former VP & General Manager of the CPU group within Arm. Co-Founder of XMOS, and currently a NED for EnSilica Plc.



**Professor Alex Yakovlev**

**Founder**

Professor of Computer System Design, Head of the MicroSystems Research Group at the University of Newcastle. Fellow of the Royal Academy of Engineering



**Dr Rishad Shafik**

**Founder**

Reader in Electronic Systems at Newcastle University. Research focusing on AI hardware design using learning automata and ultra low-power design



**Chief Technology Officer**

Former AI Deep Learning Lead at AstraZeneca. Co-founder of Manifold AI  
Joins May 2024

## Advisors



**Professor Ole-Christoffer Granmo**

**Chair Technical Steering Board**

Director of Centre for Artificial Intelligence Research at the University of Agder. Named the decade's researcher in artificial intelligence by Norwegian Artificial Intelligence Research Consortium (NORA)



**Jem Davies**

**Non-Exec Director**

Former VP and General Manager of Machine Learning and GPU groups at Arm. 35+ Years in the Semiconductor Industry



**Xavier Parkhouse-Parker**

**Chair**

CJBS alumnus. Serial Tech Entrepreneur in AI, HR & MarTech Founder. Start Up Operations Expert. CVC Capital Young Innovator 2017. COO at Cambridge Future Tech



Thank you!



A CAMBRIDGE FUTURE TECH VENTURE

Finchetto

Mark Rushworth  
CEO

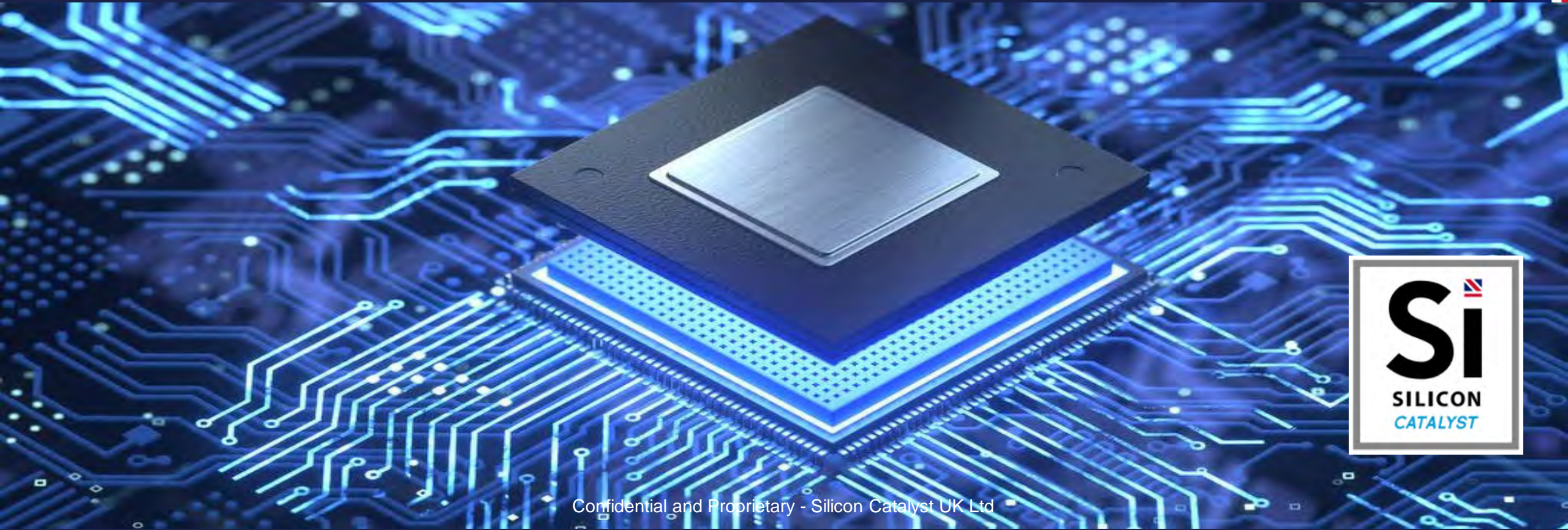


**Si** **CHIP** **START** **UK**

the semiconductor incubator  
managed by SiliconCatalyst.UK



Funded by  
UK Government





**FINCHETTO**  
SOLVING ENERGY &  
PERFORMANCE IN  
NETWORKS

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March 2024

# THE PROBLEM

## POWER



Data centres consume 2% of all global electricity



Reducing network switch energy by 90% would save:

- \$330bn in running costs
- 256MT of CO2e

## PERFORMANCE



New data creation is forecast at 50x current levels by 2035 – current telecoms networks are not able to deliver this



State-of-the-art datacoms network models are currently unrealisable due to high latency

**Lower power**

= operating costs & sustainability

**Lower latency**

= time through the network

**Faster switching time**

= quicker decision on where to send the data



## THE SOLUTION

# The world's first fully-optical, passive network switch



38W power – 26x lower power

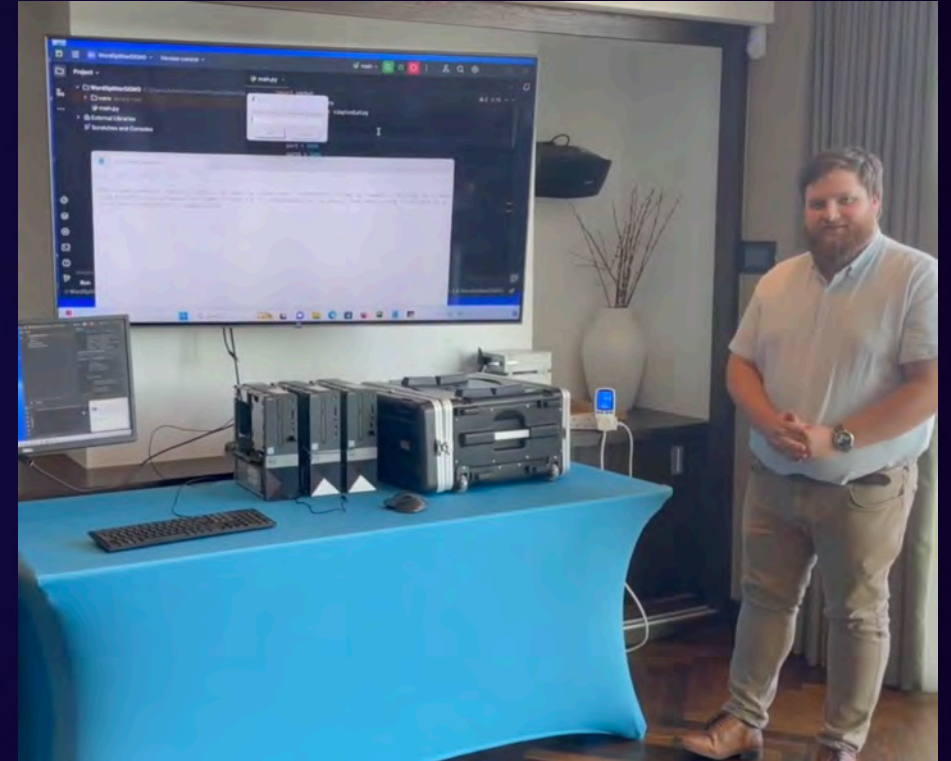


50 nanosecond latency – 40x lower latency



3-port ethernet switch – packet-switching

*vs. state-of-the-art Cisco Nexus 9232E*



# THE MARKET OPPORTUNITY

Full-product Solutions in HPC/ Datacenter and Telecommunications

DATACOMS

# 1

Future datacoms network architectures for HPC (device-level and chip-level integrated) and DCs.



\$300bn TAM

*"If we can scale this, the potential is revolutionary – this could enable the future of high-performance compute."*  
Intel

TELECOMS

# 2

Future telecoms network architectures for use initially in core (& in future, distribution & access etc.)



\$100bn TAM

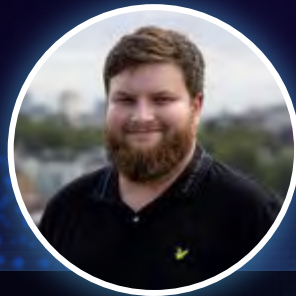
*"This technology has the potential to be a real game-changer for the telecommunications industry."* BT

# FINCHETTO SENIOR TEAM



**Mark Rushworth**  
CEO

- 2x DeepTech founder
- Qualified in integrated photonic design & characterisation



**Michael Pearcey**  
CTO

- Inventor of Finchetto's core IP
- Developer of core prototypes



**Nick Ray**  
Chair

- Tech CEO of 30 years across 4 successful exits



**Chris Cottrell**  
Telecoms Lead

- 30 years' delivering telecoms product solutions
- Cisco, HPE & Alcatel



**Jim Dertzbaugh**  
VP - US BD

- 20+ years' experience in optical switch BD
- Sales Director of Chromatis, acquired for \$4.7bn



**Bill Yost**  
Advisor

25+ years helping bring early-stage technologies to market including Polatis' optical network switch.

Core founding team of Mark & Michael, with expertise from sector-specific industry stalwarts

# BE PART OF THE FUTURE

TECH DEMONSTRATION

