

Artificial Intelligence (AI) in Hardware

"Formal Verification in the Age of Generative and Agentic AI"

The exponential rise in SoC complexity, driven by heterogeneous compute, AI acceleration, and advanced power and security architectures, has rendered simulation insufficient for first silicon success. Formal Verification (FV) proves mathematical correctness across all reachable design states, providing exhaustive coverage. Scaling FV remains challenging, demanding significant expertise to author System Verilog Assertions (SVAs) or behavioral reference models. Generative AI, Retrieval Context, and Agentic AI help broaden FV adoption, accelerating FV-Plan creation, SVA coding, constraint debugging, failure analysis, and workflow automation. Case studies on medium-complexity design blocks show the proposed AI-assisted methodology reduces the FV lifecycle from 12–20 weeks to 3–6 weeks, achieving ~70% effort reduction. Standalone LLMs improved productivity but showed requirement gaps and hallucinations. Retrieval context improved coverage and accuracy, while Agentic AI orchestrated proof execution and closure with minimal human intervention, showing clear progression in productivity and verification quality.

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