

Design Technology

"Achieving Glitch Power Visibility via Delay-Shifted Analysis for Actionable Power Optimization"

Glitch power, the dynamic power consumed by spurious signal transitions before outputs settle, is a significant contributor to total power in modern SoC designs, yet it remains invisible to conventional RTL power analysis. Industry analysts estimate that 20-40% of total dynamic power can be attributed to glitch activity in advanced designs, making glitch-aware analysis essential rather than optional. A glitch is an extra, unintended signal transition that occurs before a gate output settles to its final logic value within a clock cycle. Moreover, glitches can propagate through downstream logic, creating cascading transitions that amplify the power impact. Traditionally, capturing glitch power requires SDF annotated gate-level simulation, imposing prohibitive runtimes and repeated design verification handoffs. The result is that glitch power which can be a meaningful contributor to total dynamic power is effectively invisible to design teams during the active design cycle when optimizations can still be made. This paper presents a delay shifted waveform analysis methodology which enables glitch power estimation, including glitch generation, propagation, and configurable filtering from zero delay waveforms without SDF annotation. Prime Power takes a zero-delay input waveform from either RTL simulation or zero-delay gate-sim and dynamically adjusts the waveform edges based on the calculated arrival times derived from the gate-level netlist timing information already available in the Prime Power session. This integration does not require any changes to the simulation environment, stimulus generation, or netlist representation, thereby preserving compatibility with established verification practices. The delay-shifted methodology enables supporting multiple analysis runs within a day and thereby helping to improve design productivity. Evaluation on an advanced tech node demonstrates that delay shifted analysis captures glitch power with a fidelity approaching SDF gate-sim while reducing turnaround from weeks to hours, enabling faster iterations during power optimization flows. The practical benefit is immediate: design teams can now identify and address potential glitch power issues during the active design cycle rather than discovering them post-silicon or not at all. This represents a shift from glitch power being a post-implementation verification metric to an actionable optimization metric available during active design. This proposed methodology improves design productivity and accelerates power-efficient SoC development while reducing project risk.

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