

System Technology

"Trivializing Chip Reset Timing: A Novel Technique for SoC Backend Closure"

As System-on-Chip (SoC) designs continue to scale to hundreds of thousands of registers operating at multi-GHz frequencies, achieving reset timing closure has become one of the most persistent and resource-intensive backend design challenges. Conventional reset architectures require recovery and removal timing constraints to be closed alongside data-path setup and hold requirements, resulting in increased routing congestion, higher area and power overheads, and extended design closure cycles.

This paper introduces a novel reset synchronization architecture that fundamentally simplifies SoC reset timing closure by decoupling reset timing constraints from data-path timing. The proposed methodology transforms reset timing from a critical optimization problem into a predictable design parameter. By treating reset paths independently during physical implementation and strategically aligning clock activation after reset propagation is complete, the approach eliminates the need for conventional recovery and removal timing closure efforts.

Silicon-proven validation on a high-speed design with sub-nano second critical timing is demonstrated in STMicroelectronics 28nm FD-SOI technology. The architecture reduces recovery and removal timing violations from thousands of failing paths to zero, while achieving positive timing margins across all reset paths. In addition, it significantly lowers routing complexity, reduces implementation effort, and improves overall design robustness.

The benefits of the proposed technique scale with increasing design size, making it particularly attractive for large SoCs and next-generation chiplet-based systems. Applicable to global, local, and power-on resets, this architecture provides a low-overhead, highly scalable solution that streamlines backend implementation, accelerates design closure, and enhances reliability in high-performance, low-power semiconductor designs.

This work presents a practical and high-impact approach that enables engineering teams to focus on innovation rather than reset timing convergence, unlocking faster and more predictable SoC development.

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