

Failure Analysis Challenges and Solutions for Advanced Packaging

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Abstract

Artificial Intelligence (AI) and High-Performance Computing (HPC) applications are driving unprecedented demands for computational performance, memory bandwidth, and power efficiency. To sustain system-level scaling beyond the limitations of conventional transistor shrinkage, semiconductor manufacturers have increasingly adopted advanced packaging technologies including chiplet integration, 2.5D/3D interposer architectures, three-dimensional integrated circuits (3DIC), High-Bandwidth Memory (HBM), and Co-Packaged Optics (CPO). While these heterogeneous integration technologies provide significant benefits in terms of performance and system functionality, they also introduce substantial failure-analysis (FA) challenges. Failures may originate from multiple interconnected dies, advanced interconnect structures, packaging materials, and assembly processes that are often inaccessible using traditional analytical techniques. This paper reviews modern advanced-package architectures and examines major failure-analysis challenges associated with precision fault isolation, non-destructive high-resolution imaging, challenging sample preparation, and AI usage for effective defect detections. Representative case studies are presented to demonstrate how established FA workflows enable root-cause identification in complex package structures. Emerging challenges associated with Hybrid Bonding, Backside Power Delivery (BSPD), and Co-Packaged Optics are also discussed. The continued evolution of AI and HPC platforms will require significant advancements in FA methodologies, tools, and AI-assisted analytical workflows.

Keywords: Advanced Packaging, AI, HPC, Chiplets, Failure Analysis, Co-Packaged Optics, Fault Isolation

I. Advanced Packaging Overview

The semiconductor industry is currently undergoing a transition from traditional monolithic integration toward heterogeneous system integration. As transistor scaling becomes increasingly difficult and costly, advanced packaging has emerged as a critical technology for continuing performance growth in AI and HPC applications. Rather than placing all system functionality on a single silicon die, modern architectures distribute functionality among multiple specialized dies that are integrated within a single package.

This transition has been driven largely by the rapid growth of AI training and inference workloads, cloud computing

infrastructure, high-speed networking, and large-scale data-center applications. These applications require enormous computational throughput while simultaneously demanding improvements in energy efficiency and memory bandwidth. As a result, package architecture has become increasingly sophisticated, combining multiple processing elements, memory stacks, networking devices, and optical components into a unified advanced packaging platform.

System-in-Package (SiP) architecture provides one of the earliest examples of heterogeneous integration. By integrating multiple devices in mixed technology nodes and assembly processes within a common package, SiP solutions improve system density while enabling designers to optimize individual components independently (Fig. 1). More recently, chiplet-based architecture has further expanded system-design flexibility by partitioning large monolithic devices into smaller functional silicon building blocks. This approach provides significant advantages in manufacturing yield, product scalability, and design reuse (Figs. 2 and 3).

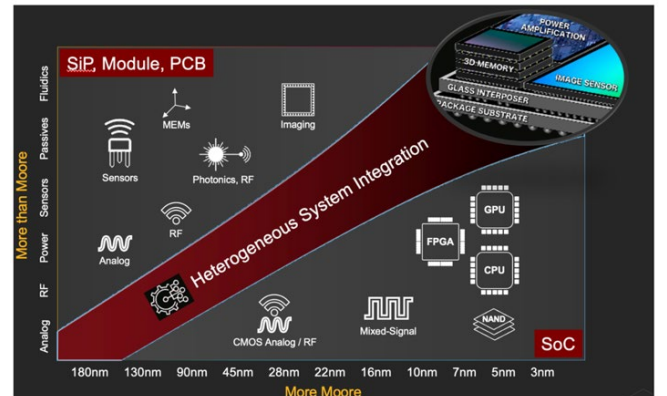


Fig. 1: Heterogeneous system integration is driven by scaling and functional diversification [1].

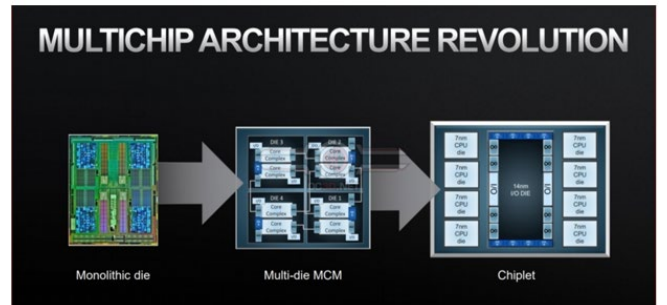


Fig. 2: Multichip architecture revolution from conventional monolithic die to multi-chip-module (MCM), and now to chiplet [2].

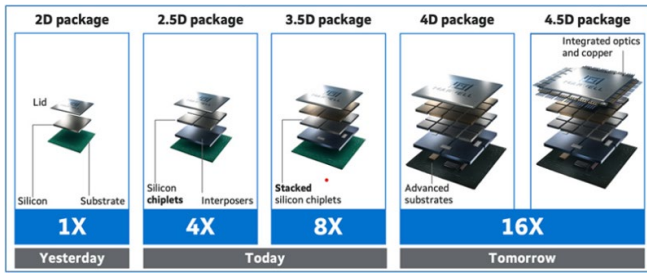


Fig. 3: Advanced chiplet roadmap from simple 2D packaging in the past to very complicated 4.5D package in the future [3].

In advanced AI and HPC systems, chiplets are frequently interconnected using 2.5D silicon interposer technologies that provide high-density interconnect pathways between compute dies and HBM stacks. Three-dimensional integration techniques further extend this concept by enabling vertical stacking of devices through Through-Silicon Vias (TSVs) and hybrid bonding structures. Emerging technologies such as co-packaged optics further increase package complexity by integrating photonic devices directly with electronic processing systems (Fig. 4).

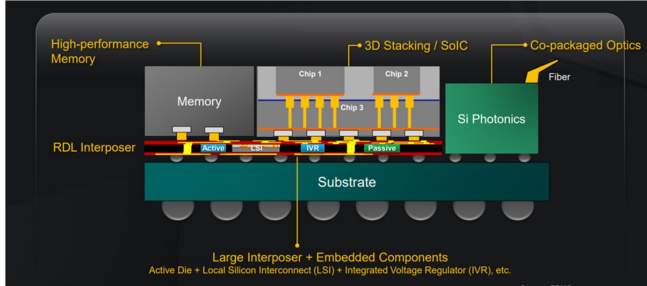


Fig. 4: Advanced packaging platform for the HPC and AI Accelerators developed by TSMC [4]

Although these advanced architectures provide substantial improvements in system performance, they also create highly complex structures containing potential failure locations distributed across multiple layers of materials and interfaces. Consequently, failure analysis must evolve beyond traditional single-die investigation techniques toward comprehensive system-level analysis methodologies.

II. Failure Analysis Challenges and Solutions

As package complexity continues to increase, failure analysis has become significantly more challenging. In conventional semiconductor devices, potential failure sites are largely confined to a single die in a simple structured package and can often be localized through established electrical and physical failure analysis techniques. By contrast, advanced packages may contain multiple active dies, memory stacks, interposers, substrates, and package-level interconnects, each introducing additional opportunities for failure.

The key reliability challenges in advanced packages include thermal management, solder joint defects,

redistribution layer (RDL) defects, interface delamination, warpage-induced failures, and stress-related damage within heterogeneous structures (Fig. 5). As the cost of failure in large AI and HPC devices continues to grow, rapid and accurate root-cause determination becomes increasingly critical [5]

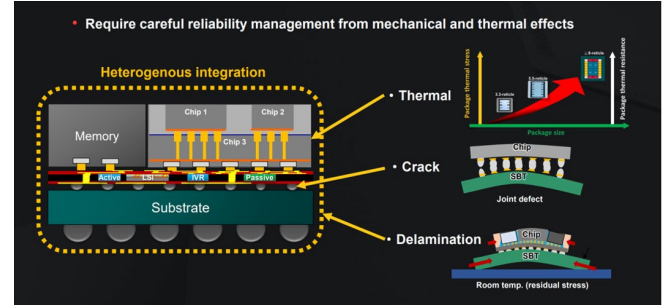


Fig. 5: Reliability challenges in advanced packaging [4]

One of the most significant failure analysis challenges is the accurate fault isolation within a complex package structure. Electrical failure symptoms frequently propagate across multiple interconnected dies, making it difficult to determine the actual physical location of the defect. A failure observed within a compute die may be caused by a defect in a micro-bump interconnect, silicon interposer, or package substrate. As package integration density increases, the distance between the observed failure manifestation and the actual root-cause location often becomes larger.

To address this challenge, advanced fault-isolation techniques need to be continuously improved. Thermal and photon emission analysis, laser-assisted localization methods, Magnetic Field Imaging (MFI), and various electrical diagnostic approaches help reduce the search area prior to destructive analysis (Fig. 6). These methods enable engineers to focus subsequent investigation efforts on specific regions within the targeted area, substantially improving analysis efficiency.

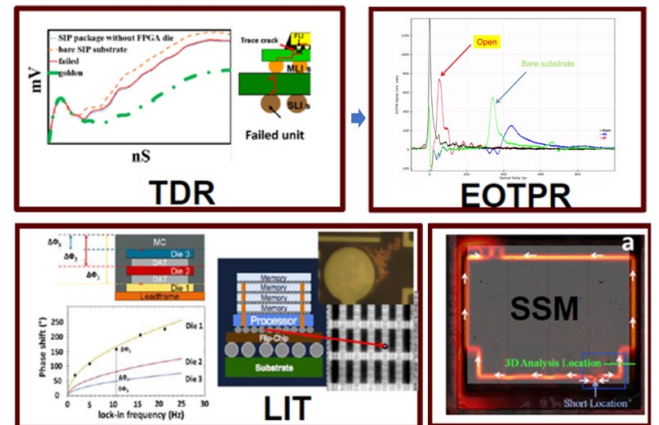


Fig. 6: Typical package level fault isolation tools and techniques [7]

Non-destructive high-resolution imaging has also become increasingly important. Because advanced packages often contain high-value devices and complex structures,

irreversible deprocessing carries significant risk. Consequently, techniques such as Scanning Acoustic Microscopy (SAM), 3D X-ray Microscopy (XRM) with micro-CT and nano-CT capability, Infrared (IR) Microscopy, and Confocal Laser Scanning Microscopy (CLSM) are now routinely used during failure investigations. High-resolution 3D X-ray imaging is particularly valuable because it enables visualization of buried structures and interconnects that are inaccessible through conventional inspection methods without requiring extensive sample preparation (Fig. 7).

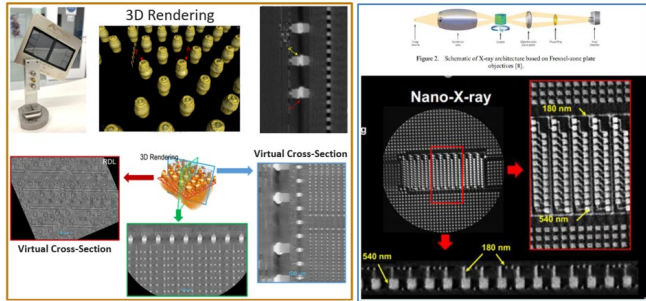


Fig. 7: 3D X-ray Microscopy (left) [3] and Nano-Tomography (right) [8]

Physical sample preparation represents another major challenge. Unlike conventional packages where simple cross-sectioning may expose the failure site, advanced packages frequently require extremely precise material removal to access deeply buried features. Precision mechanical polishing or lapping, plasma focused ion beam (FIB) milling or femtosecond laser cutting, and broad ion beam processing are now widely used to expose specific regions of interest while minimizing preparation-induced damage (Fig. 8). When combined with prior 3D X-ray CT-based localization, these methods significantly improve the probability of successfully exposing the root-cause defect.

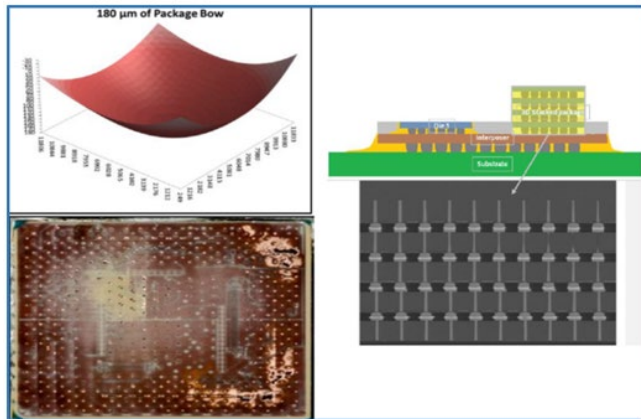


Fig. 8: Large area contour milling (left) and mechanical cross-sectioning with ion milling finish (right) [9]

Artificial intelligence is also emerging as a valuable tool for modern failure-analysis workflows. The large volume of imaging data generated during advanced package investigations can create substantial analysis bottlenecks. AI-assisted defect-recognition algorithms can automatically

identify anomalous structures, classify defects, and prioritize regions for further investigation. As package complexity continues to grow, AI is expected to play an increasingly important role in improving analytical efficiency and reducing diagnostic cycle times (Fig. 9).

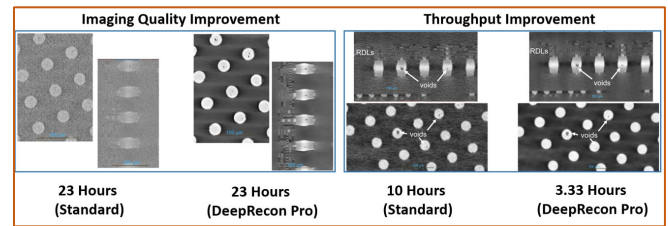


Fig. 9: High resolution 3D X-ray imaging with AI assistance on imaging quality improvement (left) and throughput time reduction (right) [3].

III. Case Studies

The following case studies demonstrate the application of advanced failure analysis methodologies to complex AI and HPC package structures.

The first case involved an ATE (Automatic Test Equipment) failure on one of the HBM stacks in a 2.5D/3D package after reliability stress testing. IR inspection revealed a white line in the bulk Si on the failing HBM stack. Large area mechanical cross-section was performed, and a long crack line was observed propagating from the top of the backside bulk Si of the affected HBM die to its active circuit areas, resulting in device failure. The cracking is suspected to originate from the package assembly process (Fig. 10).

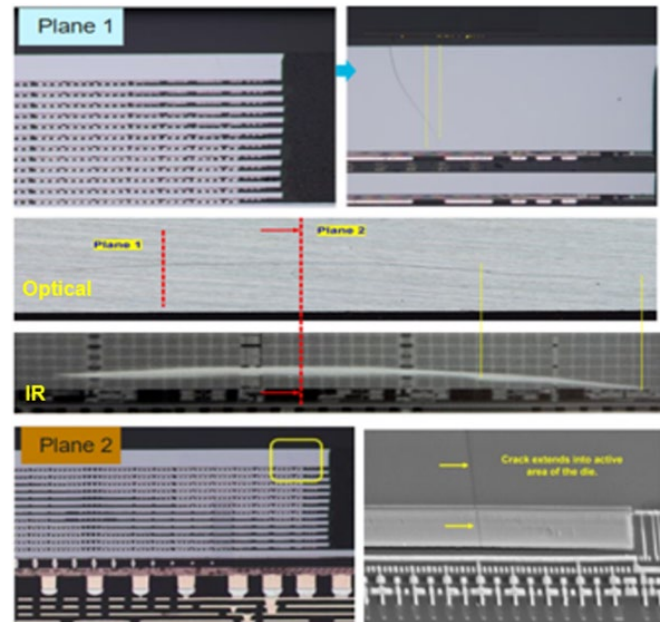


Fig. 10: ATE functional failure related to the HBM top side cracking after stress tests.

The second case study involved a die-to-die connectivity failure between the SoC and HBM dies identified during ATE

testing after assembly process. Layout search identified the failing lane at the RDL1 level in the interposer and the ubump connections to the SoC die and HBM die. The unit was then mechanically polished from the BGA package side down to the near RDL1 level of the interposer for further fault isolation. Nano-probing showed the open failure was at the ubump connection to the HBM die (Fig. 11). 3D X-ray inspection from the top view and the side view revealed an abnormal ubump at the suspected location. Plasma FIB cross-section was then performed, and the result showed a non-wetted ubump. Elemental analysis detected foreign materials at the solder joint of the non-wetted ubump, which is likely causing the non-wetting failure (Fig. 12). The information was quickly fed back to the assembly team for taking corrective actions.

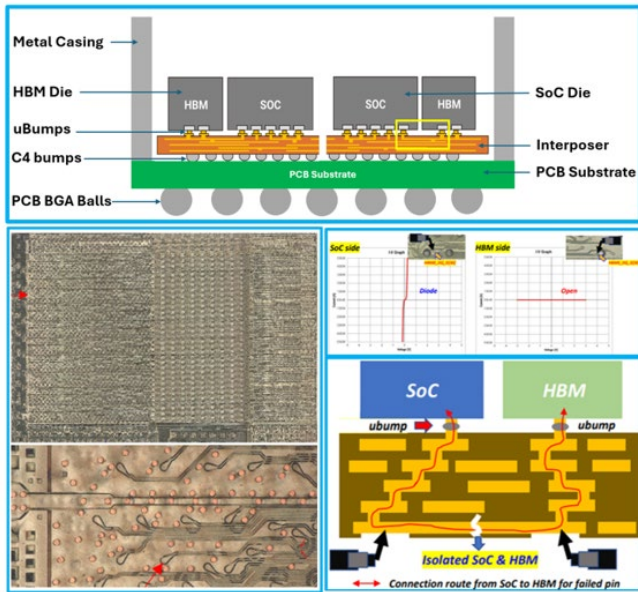


Fig. 11: An open failure was isolated at the ubump connecting to HBM that caused die-to-die connectivity failure at ATE.

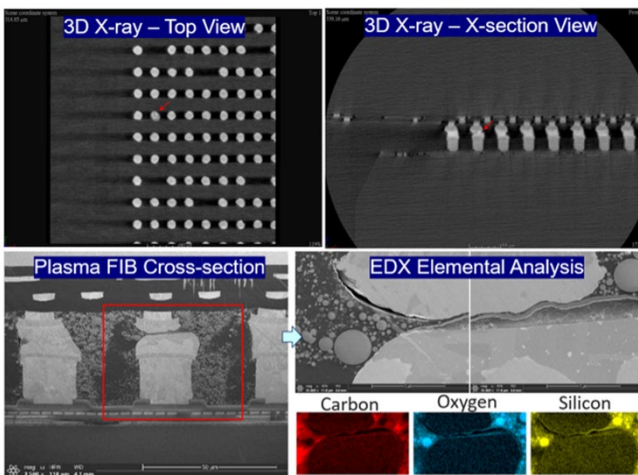


Fig. 12: 3D X-ray inspection revealed an abnormal ubump at the suspected location and PFIB cross-section confirmed non-wetted ubump due to interface contamination.

These two case studies illustrate how advanced 3D X-ray imaging, precision deprocessing, and multidisciplinary analysis techniques can successfully address the challenges associated with advanced packaging devices.

IV. New Challenges

The next generation of advanced packaging technologies will introduce additional challenges that are likely to exceed the capabilities of many existing failure analysis tools and techniques.

One emerging technology is backside power delivery. By relocating power distribution networks to the backside of the silicon wafer, designers can improve routing density and electrical performance while reducing voltage drop. However, this architectural change creates new analysis challenges because critical circuit structures become buried beneath multiple layers of thick metallization. Existing fault isolation techniques, such as Laser Voltage Imaging or Probing (LVI/LVP), are no longer useful since they need to directly interact with active transistor regions to sense circuit behavior. As a result, E-beam Probing (EBP) with FIB-assisted probe points is required to pick up the signal from active circuits, which requires extensive sample preparation and heavy capital investment (Fig. 13).

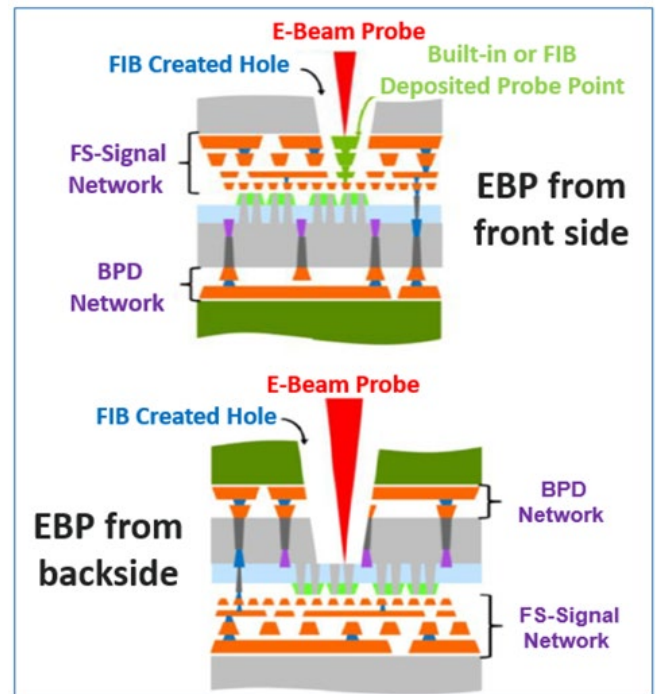


Fig. 13: Failure analysis challenges in backside power delivery devices due to blockage of backside access for fault isolation [10]

Hybrid bonding is another area of growing importance. Fine-pitch hybrid-bonded interfaces are being widely adopted for future 3D integration schemes because they provide significantly higher interconnect density than traditional ubump technologies. However, the dimensions of

these interconnect structures continue to shrink, making defects increasingly difficult to detect and characterize. Void formation, contamination, interface non-uniformity, and bonding defects may occur at scales approaching the limits of conventional inspection methods (Fig. 14).

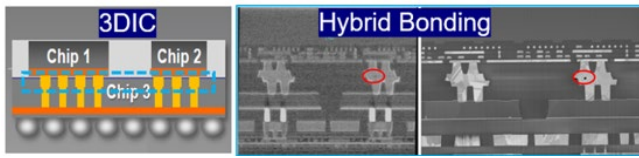


Fig. 14: Failure analysis challenges for inspecting the 3DIC devices with hybrid bonding [11]

Co-packaged optics represents perhaps the most significant departure from traditional semiconductor packaging. As electrical interconnect bandwidth approaches fundamental physical limitations, photonic communication is being integrated directly into package architectures. While this technology provides substantial system-performance advantages, it also introduces entirely new classes of failure mechanisms involving lasers, optical waveguides, photodetectors, fiber interfaces, and optical alignment structures. Failure-analysis engineers must therefore develop expertise that spans both semiconductor and photonic technologies (Fig. 15).

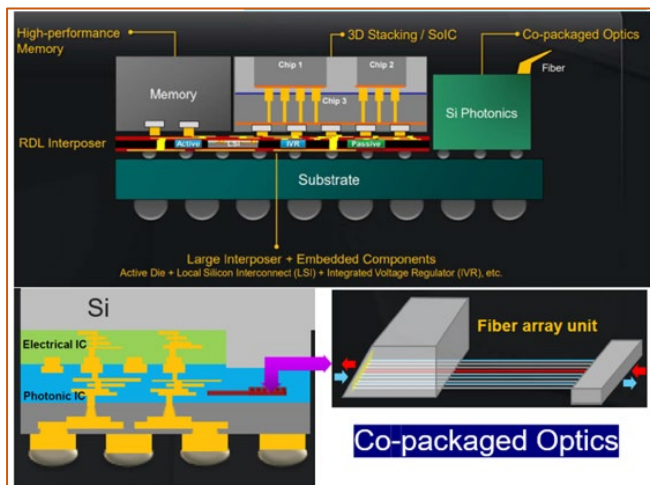


Fig. 15: New tools and techniques are required for successful failure analysis on co-packaged optics in the advanced packaging platform [4].

The growing use of artificial intelligence within manufacturing and reliability engineering will also affect future FA workflows. Machine-learning models capable of correlating electrical testing, physical imaging, manufacturing process, and reliability data may eventually enable partially autonomous root-cause determination. Such systems could dramatically reduce failure analysis cycle times while improving consistency and quality across failure investigations.

V. Conclusions

Advanced packaging technologies have become the primary enablers of future AI and HPC systems. Chiplet integration, high-bandwidth memory, silicon interposers, 3D stacking, and co-packaged optics provide unprecedented levels of performance and system integration. However, these technologies also introduce substantial challenges for reliability engineering and failure analysis.

Successfully identifying root causes within complex package structures increasingly requires a combination of advanced fault isolation, high-resolution non-destructive imaging, precision sample preparation, and sophisticated materials analysis. As demonstrated by the case studies presented in this paper, effective investigation of advanced package failures requires the coordinated use of multiple failure analysis tools and techniques within a systematic workflow.

Looking forward, emerging technologies such as backside power delivery, hybrid bonding, and co-packaged optics will continue to increase failure analysis complexity. The integration of artificial intelligence into failure analysis workflows is expected to play a critical role in addressing these challenges. Continued investment in failure analysis infrastructure, advanced characterization techniques, and AI-assisted diagnostics will be essential for ensuring the reliability and successful deployment of next-generation AI and HPC technologies.

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